SIEMENS EDA

Valor™ ODB++Design Inside for Cadence® Allegro®

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Change History

The following table contains a list of changed topics in this document.

Changes appear in this color.

Table 0-1. Change History

Topic	Comments	#Changes
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Release Notes		17
Configuration Parameter Settings		1

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Chapter 1
ODB++Design Export

ODB++Design format can capture all CAD or EDA assembly and PCB fabrication information in a single, unified file structure. ODB++Design Inside is installed as part of Cadence Allegro to allow you to export a design to ODB++Design and to view the resulting ODB++ product model.

ODB++Design Inside for Cadence Allegro contains the following components:

- **BRD2ODB translator** — Converts *.out* files, generated by Cadence Allegro, to ODB++Design version 8 or ODB++ version 7. The name of the Cadence Allegro design is contained in the names of the *.out* files. See "Generated Extract Files" on page 60.
  - If you are running the translator from within Cadence Allegro, you can specify a *.brd* file as the input path.
  - If you are running ODB++Design Inside stand-alone, you must specify a directory containing the *.out* files that have been extracted from Cadence Allegro.
- **ODB++Design Viewer** — Displays the resulting ODB++Design information, graphically. See *Valor ODB++ Viewer User Guide*.

When Allegro is to be launched from the Allegro Design Workbench, environment variable PCBDW_USER_PATH must be set when ODB++Design Inside is installed, as described in "Running the Translator from Design Workbench" on page 47.

The translator supports files from version 11 through 17.2 of these Cadence Allegro products:

- *.brd* file — From Cadence Allegro PCB Designer
- *.mcm* file — From Cadence Allegro Package Designer (APD)
- *.sip* file — From Cadence SIP

The translator does not include the option to save as the earlier ODB++ Version 6. This functionality was removed so that there is no confusion over what should be sent to manufacturing. Manufacturers must use a software version capable of reading ODB++ Version 7 or ODB++Design Version 8 format. Mentor Graphics Frontline applications such as Genesis work with a variation of the ODB++Design format, but they can import and use the ODB++ Version 7 and the ODB++Design Version 8 format.

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Translating a Design to ODB++Design Format

You use the ODB++Design Inside for Cadence Allegro translator to specify parameters and to run the translation, to export a Cadence Allegro design to an ODB++ product model.

Prerequisites

Perform these tasks as necessary:

- Set configuration parameters. See "Configuration Parameter Settings" on page 47.
- Set environment variables. See "Setting Environment Variables" on page 54.
- Configure thermal models. See "Thermal Model Configuration" on page 55.

Procedure

1. Open ODB++Design Inside from within Cadence Allegro or stand-alone:
   - From within Cadence Allegro, choose **File > Export > ODB++Design Inside** or click  .
   - Use a line mode command to activate the stand-alone translator:
     - Windows:

       ```
       "%ALLEGRO_BRD2ODB%/brd2odb.exe" -gui
       ```

     - UNIX:

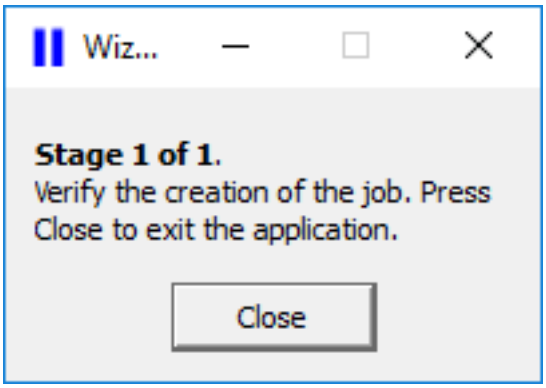
       ```
       $ALLEGRO_BRD2ODB/brd2odb -gui
       ```

     See "Command Line Parameters" on page 69.
2. Specify the information described in "Specifying File Options and Output Options Page" on page 15.
   - If you are running ODB++Design Inside from within Cadence Allegro, you can specify a *.brd* file as the input path.
   - If you are running ODB++Design Inside stand-alone, you must specify a directory containing the *.out* files that have been extracted from Cadence Allegro. See "Generated Extract Files" on page 60.
3. If you have selected Export Option = Partial, specify the partial export parameters as described in "Specifying Partial Export Parameters Page" on page 19.
4. If you have selected Show more options = Yes, specify the information as described in "Specifying Additional Parameters Pages" on page 21.
5. Click **Next** on the last page of parameters to perform the translation.
6. If you want to restart the wizard and re-enter the options, click **Setting > Reset Wizard**.

Results

The product model is written in ODB++Design format to the specified location.

If you have selected Open ODB++Design viewer = Yes, the ODB++Design Inside wizard pauses and displays the message Verify the creation of the job. Press Close to exit the application:



ODB++Design Viewer opens, displaying the product model as described in *Valor ODB++ Viewer User Guide*.

Saving the Configuration

If you will be using the same configuration parameters for several translations, you can save the configuration to a file.

You can save the configuration to the standard user location, to the standard system location, or to another location. The user-level configuration, if it exists, is loaded when ODB++Design Inside starts. Otherwise, the system-level configuration is used to supply default values for the wizard.

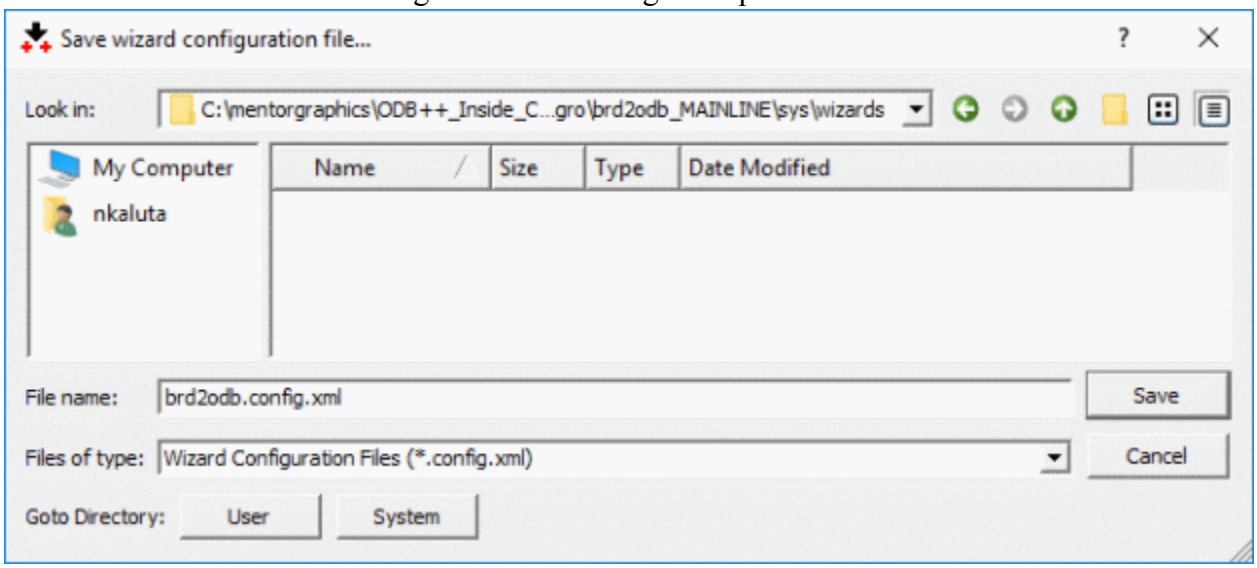
Prerequisites

Run the ODB++Design Inside wizard as described in "Translating a Design to ODB++Design Format" on page 8.

Procedure

1. Choose **Setting > Save Config**.

The Save wizard configuration file dialog box opens.



2. Specify the parameter values:

Parameter	Description
Look in:	The directory in which to save the configuration file. This can be the standard user location or the standard system location, or another location. • To store files at the user location, click the **User** button. The user location is displayed in this field. If there is a file saved at the user location, it is loaded when ODB++Design Inside opens. • To store the file at the system location, click the **System** button.The system location is displayed in this field. This configuration is loaded when ODB++Design Inside opens, if there is no configuration file in the user location. • You can save the configuration file in another location. To use the parameter settings, copy the file to the standard name, in either the user location or the system location, before opening ODB++Design Inside.
File name	The file name to which to save the configuration. If you are storing the file at the user location or at the system location, and you want the wizard to load the default values from this file on startup, save the configuration to the standard file name: *brd2odb.config.xml*. If you are storing the configuration at a different location, to a file that will be copied to the user location or the system location as needed, you can specify any file name.

Parameter	Description
Files of type	If you are storing the file at the user location or at the system location, leave the default file type.

Editing the Matrix File

If necessary, you can edit the information about the layers that were extracted from the Cadence Allegro design. For each layer you can edit the context, type, polarity, and side.

The options of the matrix file editor are equivalent to the options on the Artwork Control Form dialog box of Cadence Allegro.

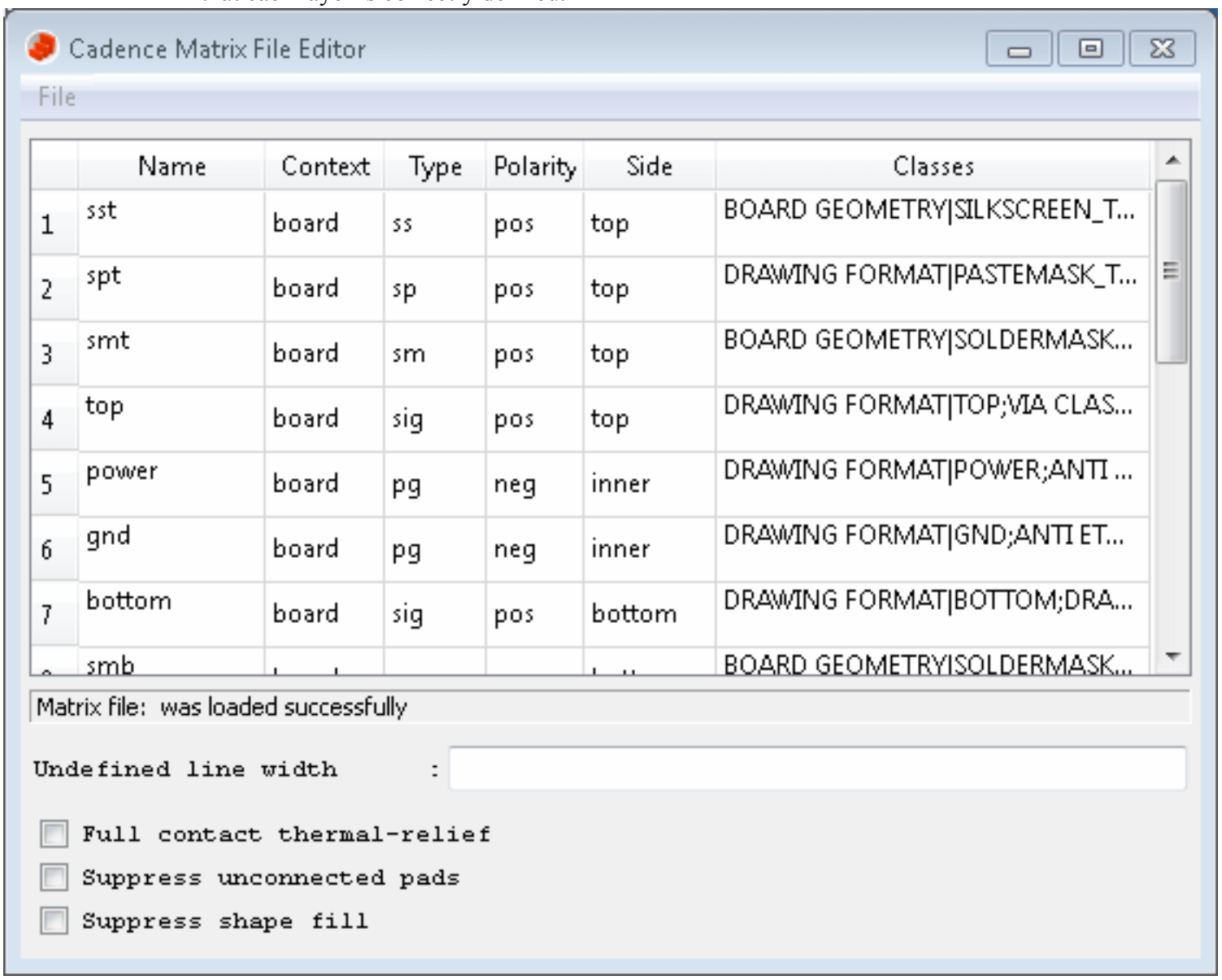
Layers are translated according to the data taken from the files *layers_<product_model>.out* and *films_<product_model>.out*. It is not unusual to find data for copper layers mixed with document layers.

The translator designates the top and bottom layers according to the pairs of class | sub-class ETCH|<*layer_name*>. If several layers contain these pairs, the first one found is used. To avoid the mixing and duplication of layer data, it is necessary to edit the matrix file before translation.

The first time a design is translated, it does not usually contain a matrix file.

Procedure

1. Use the drop-down lists in the Cadence Matrix File Editor window to edit parameters so that each layer is correctly defined.



- If you change a top or bottom layer to a document layer, its name is changed to what it was originally.
- If you change a document layer to a signal layer, its name is assigned according to the ETCH sub-class found in it.

Make sure that changes to layers remain synchronized. For example, signal must be assigned side = top or bottom and power and ground layers must be side = inner. They cannot be of context misc. Document layers must be assigned side = auto and polarity = pos. Unsynchronized data causes incorrect translation.

2. Set options for thermal relief, unconnected pads, and shape fill for each layer.

Option	Explanation

Full contact thermal-relief	Controls the creation of thermal symbols on a specific layer.
	• selected — Suppresses the creation of thermal symbols.
	• cleared — Creates thermal symbols, if they are defined, in this way:
	  • If there are *<thermal symbol name>.outdra* files, thermal symbols are added as defined in these files.
	  • If there are no *outdra* files, and Use thermal model file = Use file was specified in the wizard, the thermal model specified in Set filename of thermal model is searched. If there are thermal symbols defined there, they are added.
	The file *valor_ex.il* creates ASCII files named *<thermal symbol name>.outdra* if there are DRA files with the design. These files are used to create thermal symbols. Each file defines one thermal symbol. Only the thermals for which there are *outdra* files are replaced.

Suppress unconnected pads	Controls whether unconnected pads are suppressed for the selected layer.
Suppress shape fill	Controls the creation of the laminate area for the selected layer during translation. • selected — Creation of the laminate area is suppressed. The design must have filled areas replaced with separation lines in Power & Ground layers. • cleared — By default, text on P&G layers is translated with negative polarity. This reads product models in the same way the -s switch is used in the Allegro Artwork command. The laminate area is created for all negative layers by creating a single surface consisting of the board outline (filled) with all split plane areas subtracted from it. Creation of the laminate area in ODB++ is equivalent to the "shapefill" algorithm in Allegro (the -s switch is used to suppress the shapefill algorithm).

3. Choose **File > Save** to save the corrections. You can specify the edited matrix file in Matrix file so that the translation creates layers according to the file.

ODB++Design Inside Wizard Pages

The ODB++Design Inside wizard comprises a set of pages that lead you through the translation stages: setting the file options and output options, configuring partial output, setting additional translation parameters, and running the translation.

The pages are listed in order of execution of the wizard stages:

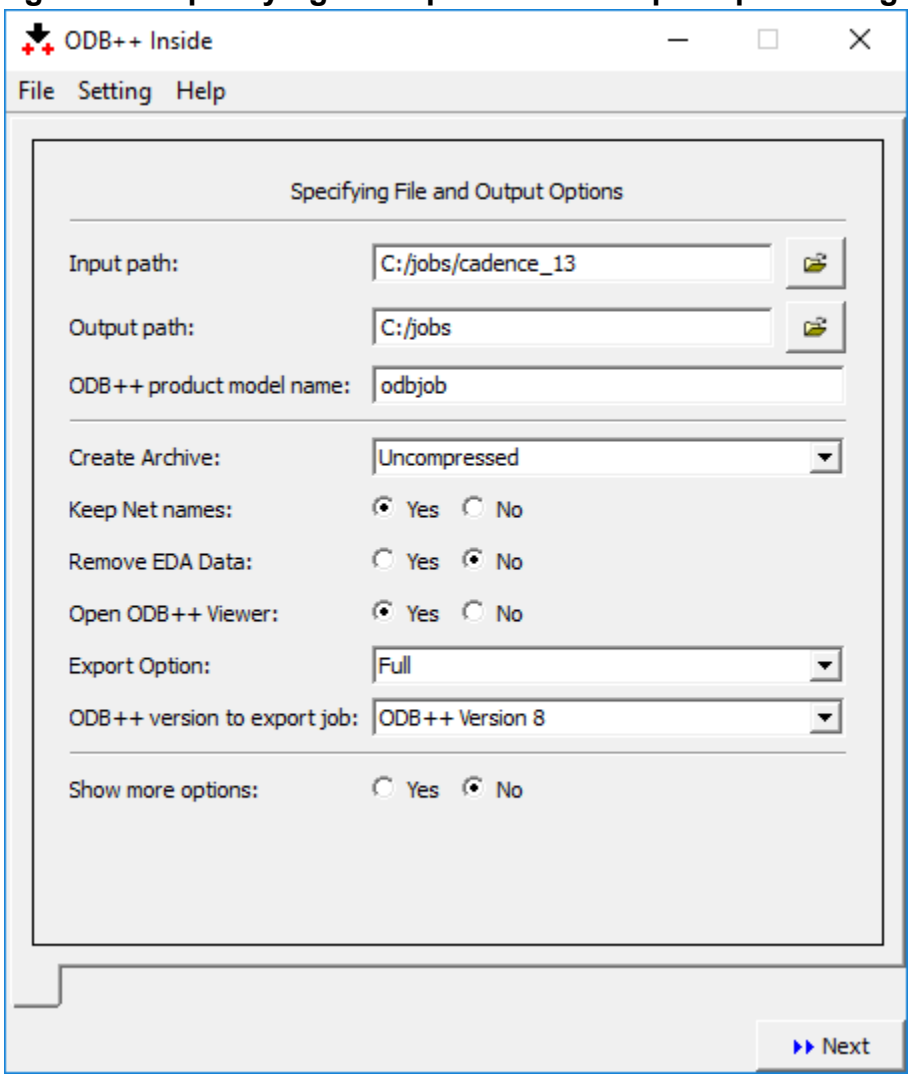
Specifying File Options and Output Options Page **15**
Specifying Partial Export Parameters Page **19**
Specifying Additional Parameters Pages **21**

Specifying File Options and Output Options Page

You access this page while performing Step 2 of the procedure "Translating a Design to ODB++Design Format".

You must provide input and output paths and output options needed by the translator, and select actions to be performed by the translator.

Figure 1-1. Specifying File Options and Output Options Page



Objects

Table 1-1. File Options

Object	Description
Input path	The input path of the Allegro design. Click  to browse to a file or a directory. If you are running ODB++Design Inside from within Cadence Allegro, you can specify a *.brd* file as the input path. If you are running ODB++Design Inside stand-alone, you must specify a directory containing *.out* files that have been extracted from Cadence Allegro. See "Generated Extract Files" on page 60.
Output path	The path for the ODB++ output. Click  to browse to a file or a directory.
Output product model name	The name of the ODB++ product model to be created.

Table 1-2. Translator Actions

Field	Description
Create Archive	Controls the format of the ODB++ output. • **Uncompressed** (default) • **Tar** — Compresses the ODB++ folders into a tared file. • **Tar gzip (.tgz)** — Compresses the ODB++ folders into a tared and zipped *tgz* file.
Keep Net names	Controls whether net names are renamed numerically or are kept as their original names.
Remove EDA Data	Removes component/package data.

Table 1-2. Translator Actions (cont.)

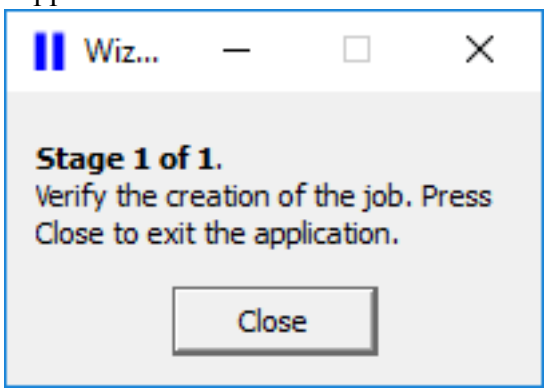
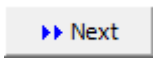
Field	Description
Open ODB++Design Viewer	Opens the ODB++Design Viewer application to display the imported design, when the translation completes. The ODB++Design Inside wizard remains open, but is paused. The wizard displays the message Verify the creation of the job. Click **Close** to exit the application.  The ODB++Design Viewer opens, displaying the resulting ODB++ data. To close ODB++Design Viewer and the ODB++Design Inside wizard, perform one of these tasks: • Choose **File > Exit** to close the ODB++Design Viewer. • In the Wizard Paused message box, click **Close**. If your examination of the ODB++ data indicates that you need to change import parameters, you can click **Setting > Reset Wizard** in the ODB++Design Inside wizard to restart the wizard. If you have saved your configuration, you only need to enter the parameters that need to be changed. See *ODB++Design Viewer User Guide*.

Table 1-2. Translator Actions (cont.)

Field	Description

Export Option	Controls how much data is exported to ODB++:
	• **Full** — All information in the design Export Fabrication.
	• **Partial** — You can select which data is exported. See "Specifying Partial Export Parameters Page" on page 19.
	• **FAB** — Exports layers and data options for fabrication:
	  • Physical nets - output for net points
	  • Outer copper layers
	  • Silk Screen layers
	  • Solder Paste layers
	  • Solder Mask layers
	  • Drill / Rout layers
	  • Document layers
	  • Inner layers
	• **ASSY** — Exports layers and data options for assembly:
	  • Components/Packages & Logical nets - components + logical nets (net nodes/net attributes/net properties)
	  • Physical nets - output for net points
	  • Outer copper layers
	  • Silk Screen layers
	  • Solder Paste layers
	  • Solder Mask layers
	  • Drill / Rout layers
	  • Document layers

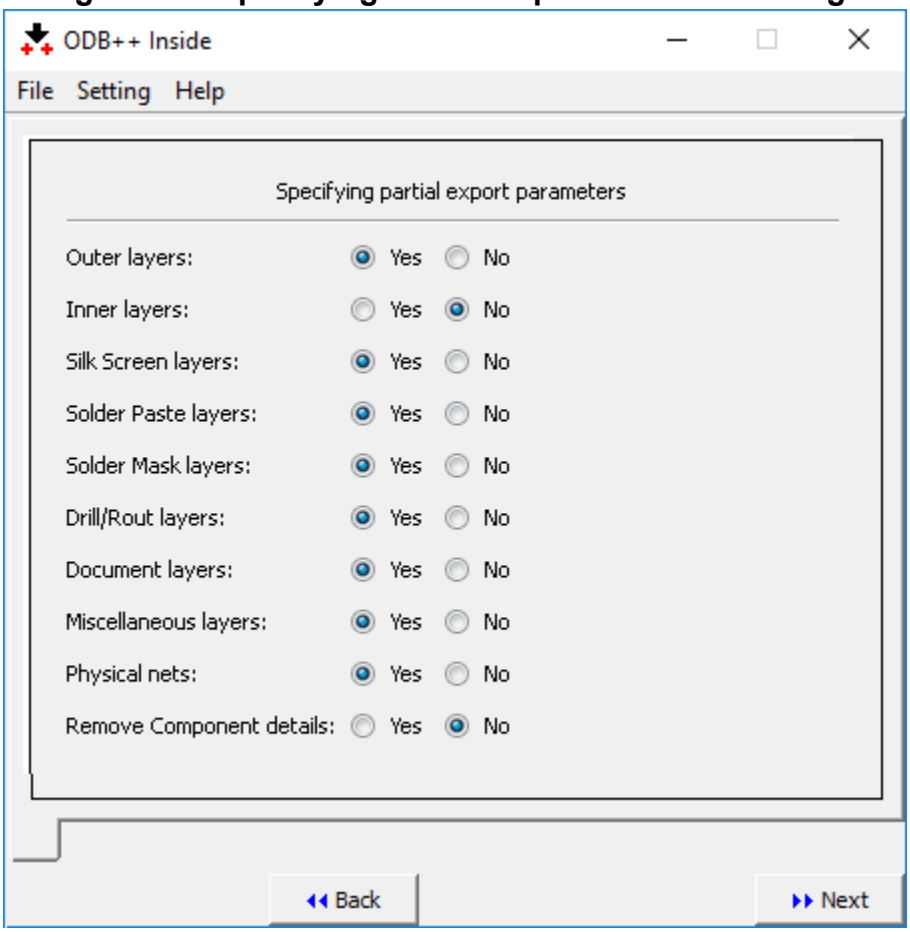
ODB++Design version to export job	One of these ODB++Design versions: • ODB++Design Version 8 • ODB++ Version 7
Show more options	Activates the options for setting additional parameters as described in Table 1-3 through Table 1-6.
Next 	Does one of the following: • If you selected **Export Option** = **Partial**, displays Specifying Partial Export Parameters Page. • If you selected **Export Option** ≠ **Partial** AND **Show more options** = **Yes**, displays Specifying Additional Parameters Pages. • If you selected **Export Option** ≠ **Partial** AND **Show more options** = **No**, runs the translation.

Specifying Partial Export Parameters Page

You access this page while performing Step 3 of the procedure "Translating a Design to ODB++ Format".

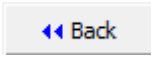
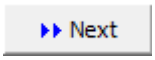
You can specify which information should be extracted from the design.

Figure 1-2. Specifying Partial Export Parameters Page



Objects

Object	Description
Outer layers	Yes / No Controls whether to include the outer layers in the ODB++ product model.
Inner layers	Yes / No Controls whether to include the inner layers in the ODB++ product model
Silk Screen layers	Yes / No Controls whether to include the silk screen layers in the ODB++ product model.

Object	Description
Solder Paste layers	Yes / No Controls whether to include the solder paste layers in the ODB++ product model.
Solder Mask layers	Yes / No Controls whether to include the solder mask layers in the ODB++ product model.
Drill/Rout layers	Yes / No Controls whether to include the drill/rout layers in the ODB++ product model.
Document layers	Yes / No Controls whether to include the document layers in the ODB++ product model.
Physical nets	Yes / No Controls whether to include the net names in the ODB++ product model.
Miscellaneous layers	Yes / No Controls whether to include the miscellaneous layers in the ODB++ product model.
Remove component details	Yes / No Controls whether to exclude attributes and properties of the components from the ODB++ product model.
Back 	Displays the Specifying File Options and Output Options Page.
Next 	Does one of the following: • If you selected **Show more options** = **Yes**, displays the Specifying Additional Parameters Pages. • If you selected **Show more options** = **No**, runs the translation.

Specifying Additional Parameters Pages

You access these pages while performing Step 4 of the procedure “Translating a Design to ODB++ Format.”

You can specify additional and configuration parameters.

Description

Figure 1-3. Specifying Additional Parameters - Page 1

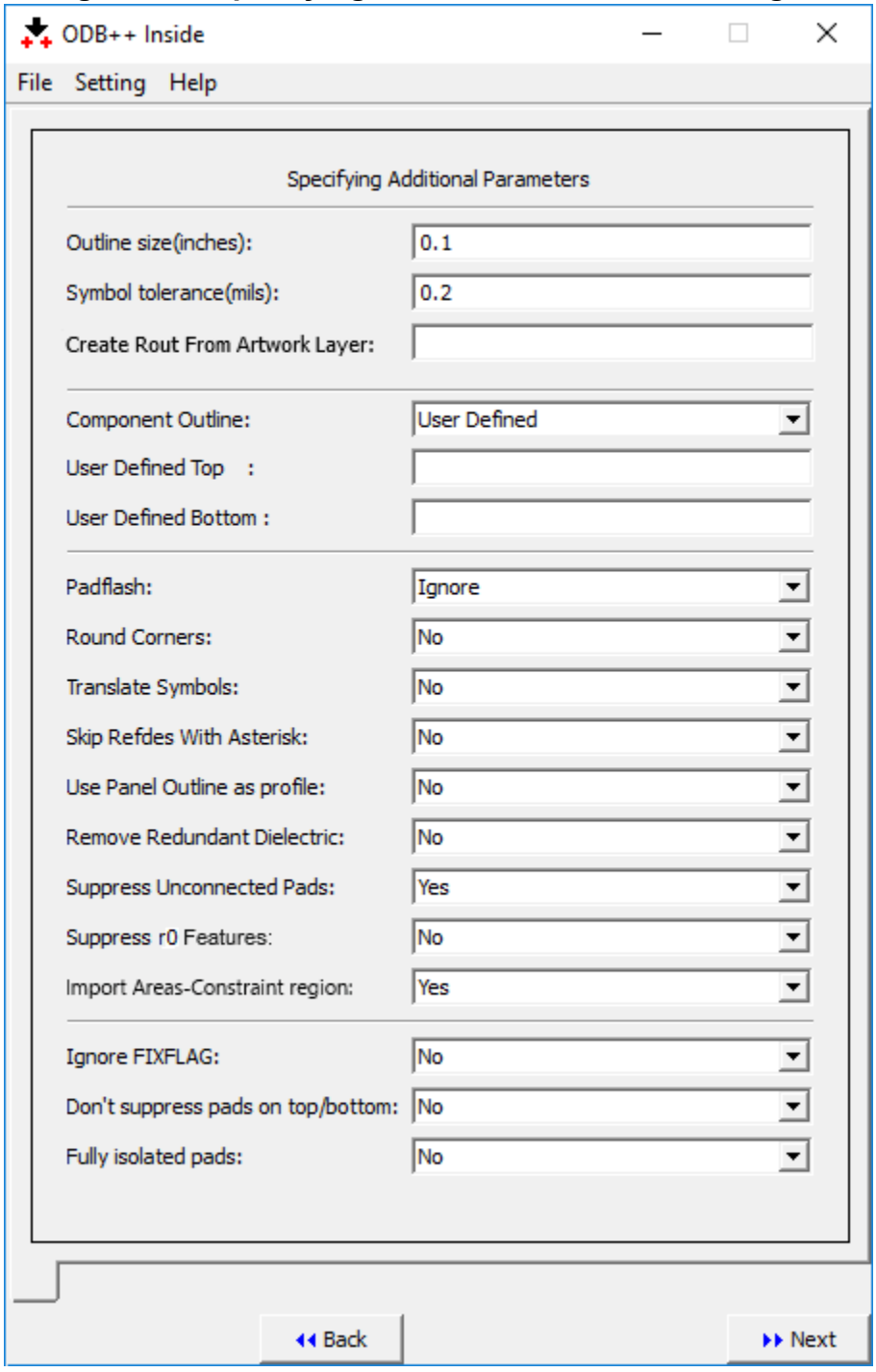


Figure 1-4. Specifying Additional Parameters - Page 2

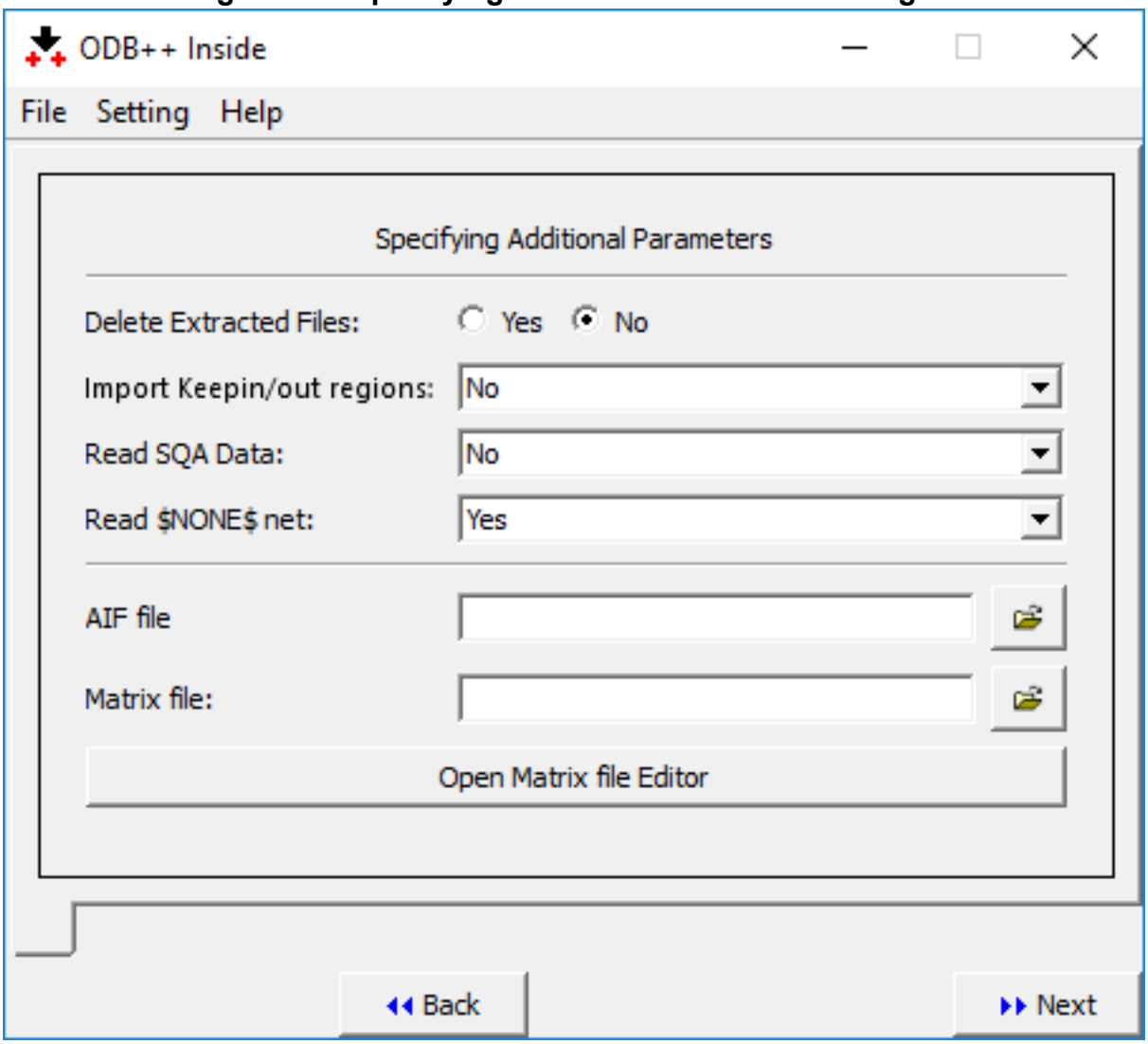
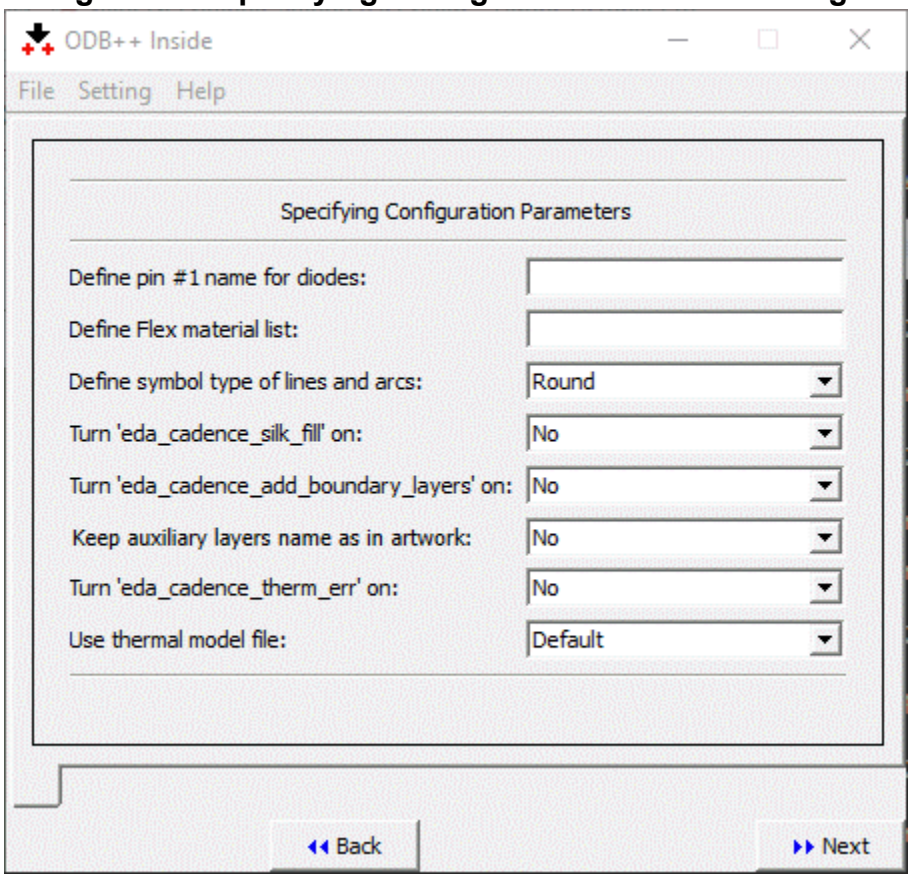


Figure 1-5. Specifying Configuration Parameters Page



Objects

Table 1-3. Specifying Additional Parameters - Page 1

Object	Description
Outline size (inches)	When creating negative plane layers, the size of the frame is the value of this parameter. For accurate translation this value should match the -o option in the Cadence Allegro artwork program. If these two parameters differ, the frame will be created according to the value in Outline size. The value is in inches. The field allows a precision of up to four digits. For example, 0.4321.

Table 1-3. Specifying Additional Parameters - Page 1 (cont.)

Object	Description
Symbol tolerance (mils)	The system compares shapes that are input, with symbols previously input in the same session, and with standard and semi-standard system symbols. • 0 — only if the input shape exactly matches a system symbol, is the system symbol used. If it does not match, the input shape is used "as is" without change. • positive value — the input shape is compared to system symbols within the tolerance specified. If it can be matched, the system symbol is used. Use this parameter as appropriate for the type of file you expect to input. The lower the tolerance the more critical the system is in judging that shapes are equivalent. The value is specified in mils. The field allows a precision of up to four digits. For example, 0.2134.
Create Rout From Artwork Layer	Controls how the rout is created: • If the field contains the name of a valid layer, as specified in the Allegro artwork, the features in that layer are used to create an ODB++ rout layer with the original name. • If this field is empty, or the value is not found in the *.out* files, the translation creates a rout layer by merging the features from the following Allegro artwork CLASS/SUBCLASS: BOARD GEOMETRY:OUTLINE"&"BOARD GEOMETRY:DESIGN_OUTLINE"&"BOARD GEOMETRY:CUTOUT Related line mode command switch is -ral. See "Command Line Parameters" on page 69.

Table 1-3. Specifying Additional Parameters - Page 1 (cont.)

Object	Description
Component Outline	Controls how the component outline is created. • **Placebound** — (Recommended) When place bound shapes are available (PART GEOMETRY sub-classes PLACE_BOUND_TOP and PLACE_BOUND_BOTTOM) they are used for the component outline. Otherwise, the limits of the assembly features are used. • **Assembly**— The limits of the assembly features are used. A heuristic algorithm attempts to determine the actual component outline from the collection of data on the sub-classes ASSEMBLY_TOP and ASSEMBLY_BOTTOM of the package geometry. This may result in an unexpected component outline if the data defining it is not complete in terms of ODB++, that is, a well defined closed polygon. • **DFA** — If DFA boundaries data exists, the component outline is taken from the PART GEOMETRY sub-classes DFA_BOUND_TOP and DFA_BOUND_BOTTOM. Otherwise, pin bounding boxes are used. • **User Defined** — The component outline is taken from the sub-classes entered into User Defined Top and User Defined Bottom.
User Defined Top User Defined Bottom	Available only when Component Outline = User Defined. Specify the top and bottom subclasses from which the component outline is taken. These fields must be set with the values specified in the component subclasses file. See “Deriving Component Outline From Specific Subclasses” on page 80.

Table 1-3. Specifying Additional Parameters - Page 1 (cont.)

Object	Description

Padflash	Allegro pad definitions can have padflash codes that override the pad size information for the padstack. This information is extracted into the twelfth field of the pad extract file (*pads_<brd name>.out*).
	For instance, on fiducials, a designer defines a padstack called FID120RD40RD that appears in Allegro as a 120 mil diameter pad with a 120 mil diameter solder mask. It also has a padflash definition of RD40.
	• **Ignore** — (default) The Padflash field is ignored and instead, the pad size is used. In the example, the example padstack would be constructed of 120 mil diameter pads during EDA translation.
	• **Substitute (Ignore missing)** — (recommended) Sets the Padflash definition using the following method:
	  • If the Padflash code exists and the *thermal_models* file using Cadence Allegro padflashes exists, the name in the PADFLASH field is used in conjunction with the thermal models file to determine what is placed at the location. In the example, the PADFLASH name RD40 would determine the actual fiducial on the copper layer based on the current thermal model.
	  • In other cases, the configuration parameters eda_cadence_read_dra and eda_cadence_therm_err control the translator behavior:
	  eda_cadence_read_dra = yes — The file <*thermal symbol name*>*.outdra* is read (if exists) during translation, providing the PADFLASH symbol definition.
	  eda_cadence_read_dra = no — The file <*thermal symbol name*>*.outdra* is ignored.
	  eda_cadence_therm_err = no — If the Padflash does not exist in the *thermal_models* file or as an *outdra* file, the original pad size is used.
	  eda_cadence_therm_err = yes — If the Padflash does not exist in the *thermal_models* file or as *outdra* file, the translation fails with a message listing the padstack name.

Round Corners	Indicates whether corners should be rounded. • **No** — (default) process precise (square) corners. • **Yes** — round corners of polygons (contours).
Translate Symbols	Indicates whether symbols should be translated as components. • **Yes** — (default) symbols are translated as components. If there are multiple shapes, each will be translated as a separate component. • **No** — symbols are not translated.

Table 1-3. Specifying Additional Parameters - Page 1 (cont.)

Object	Description
Skip Refdes With Asterisk	Controls whether components with names containing an asterisk (*) should be translated. • **No** — All components are translated. (default) • **Yes** — Components with names containing an asterisk are not translated. • **Part** — The translation excludes components whose RefDes contains an asterisk (*) but includes their pad and drill features.
Use Panel Outline as profile	Controls which data in the *geoms_<pm>.out* file is used to define the step profile: • **No** — Lines with SUBCLASS = PANEL/PANEL_OUTLINE provide the step outline. • **Yes** — Lines with SUBCLASS = DESIGN_OUTLINE/OUTLINE provide the step outline. Related line mode command switch is -up. See "Command Line Parameters" on page 69.
Remove Redundant Dielectric	Controls whether successive dielectric layers are combined: • **No** — (default) Combines successive dielectric layers. • **Yes** — Does not combine successive dielectric layers, which may result in the wrong calculation of back drill spans. Related line mode command switch is -rrd. See "Command Line Parameters" on page 69.
Suppress Unconnected Pads	Controls whether unconnected pads are included in the translated design if the Allegro design contains the following: • In the films file, SUPPRESS_UNCONNECTED_PADS = Yes. • In the pads extract file, FIXFLAG = o (optional). If FIXFLAG = f (fixed), it can be ignored by selecting Ignore FIXFLAG. This sets configuration parameter eda_cadence_suppress. Pads on negative layers and pads associated with embedded components are never suppressed. • **Yes** — Unconnected pads are not translated. This option activates the advanced suppressing options listed in Table 1-4. • **No** (default) — Unconnected pads are translated. Related line mode command switches are -iff, -bb, -fi, and -ups. See "Command Line Parameters" on page 69.
Suppress r0 Features	Controls whether to suppress the creation of r0 lines and arcs on copper and solder layers.

Table 1-3. Specifying Additional Parameters - Page 1 (cont.)

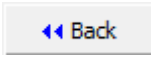
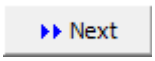
Object	Description
Import Areas-Constraint region	When set to Yes, triggers the generation of a single ODB++ product model layer by the name of "fab_drc." The layer is generated based on the Allegro layer group called Constraint region. Related line mode command switch is -rr. See "Command Line Parameters" on page 69.
Back 	Does one of the following: • If you selected **Export Option** = **Partial**, displays the Specifying Partial Export Parameters Page. • If you selected **Export Option** ≠ **Partial**, displays the Specifying File Options and Output Options Page.
Next 	Displays Page 2 of Specifying Additional Parameters. See Table 1-5.

Table 1-4. Specifying Additional Parameters - Suppress Unconnected Pads

Object	Description
Prerequisite: Suppress Unconnected Pads = Yes (See Table 1-3) **Note:** The following options are available to control which pads are suppressed, unless you are using options in Cadence Allegro V16.2 to control how to treat unconnected pads, and you access the translator from within Allegro.	
Ignore FIXFLAG	Ignores the setting of FIXFLAG in the pads extract file.

Table 1-4. Specifying Additional Parameters - Suppress Unconnected Pads

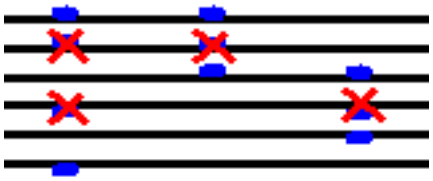
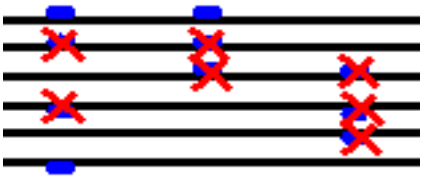
Object	Description
Don”t suppress pads on top/bottom	Controls whether unconnected pads at the top and bottom of a drill are suppressed. Available only if Suppress Unconnected Pads = Yes. • **Yes** — Unconnected pads at the top and bottom of a drill are not suppressed. (All unconnected pads other than those on the top and bottom of a drill are suppressed)  • **No** (default) — Unconnected pads at the top and bottom of a drill are suppressed. (All unconnected pads other than those on the top and bottom layers of a board are suppressed.) 

Table 1-4. Specifying Additional Parameters - Suppress Unconnected Pads

Object	Description

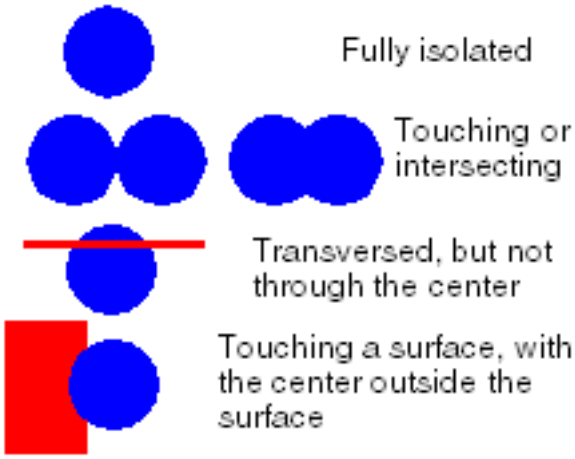
Fully isolated pads	Controls which pads are considered to be unconnected. Available only if Suppress Unconnected Pads = Yes.
	• **Yes** — Only single pads, touching no other feature on the layer, are considered to be unconnected.
	 
	
	• **No** — (default) All of these pads are considered to be unconnected:
	  • A single totally isolated pad.
	  • Two pads touching or intersecting.
	  • A pad transversed by a trace not through its center.
	  • A pad touching a surface where its center is not inside the surface.
	 

Table 1-5. Specifying Additional Parameters - Page 2

Object	Description
Delete Extracted Files	Controls whether temporary extract files created during translation are deleted.
Import Keepin/out regions	When set to Yes, triggers the generation of multiple DRC layers beginning with the prefix “drc_”. • Allegro layers Route keepout, Route keepin and Via keepout are used to generate an ODB++ layer called drc_route. • Allegro layers Package keepout, Package keepin, Component keepout and Component keepin are used to create drc_comp_top and drc_comp_bottom. • Allegro layers No_Probe_Top and No_Probe_Bottom are used to create drc_tp_top and drc_tp_bottom.

Table 1-5. Specifying Additional Parameters - Page 2 (cont.)

Object	Description
Read SQA Data	Controls whether Signal Quality Analysis data should be read. • **Yes** — SQA data is read and a signal quality layer is created. • **No** — A signal quality data layer is not created and the tech file is not read. The translation takes less time.
Read $NONE$ net	Controls whether to assign features with no net to the $NONE$ net. • **Yes** — Assign features with no net to the $NONE$ net (default). • **No** — Do not assign features with no net to the $NONE$ net.

Matrix file	To indicate the matrix file to use, perform one of these actions:
	• To use the matrix file generated from the product model, leave this field empty.
	• To use an existing matrix file, type the full path to the file.
	• To edit the matrix generated from the product model, and use the edited matrix file, perform these actions:
	  • Click **Open Matrix file Editor** to open the Cadence Matrix File Editor. Edit the file and save it. See "Editing the Matrix File" on page 11.
	  • Type the full path to the matrix file in the Matrix file field.

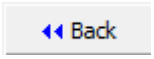
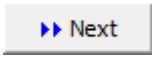
AIF File	HDI net information can be translated, and can be used to perform HDI net validation. By default, an AIF file residing in the same folder as the *out* files is used during translation. If your AIF file is located in a different folder, specify the location in the AIF File box. This location is used for subsequent translations even if there is an AIF file in the same folder as the *out* files, so be sure and change this location for subsequent translations if necessary. Make sure that you are using the current Skill script. Before opening Cadence Allegro to export information, copy the current script to the Cadence directory from this location: *<installation folder>\all\eda\cadence\set_allegro*
Back 	Displays Page 1 of Specifying Additional Parameters. See Table 1-3.
Next 	Displays the Specifying Configuration Parameters Page. See Table 1-6.

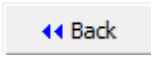
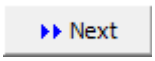
Table 1-6. Specifying Configuration Parameters Page

Object	Description
Define pin #1 name for diodes	Lists the names of diode leads that will be designated as pins #1. Multiple values are separated by semicolons (;). Sets configuration parameter diodes_pin1_name. For example, if you want to designate all leads named “K” and “C” as pins #1, type the following values: K;C
Define Flex material list	Lists the names of flexible dielectric materials. Multiple values are separated by semicolons (;). For example: POLYIMIDE;POLYIMIDE_FILM At import of Cadence Allegro data, the copper layers below and above a dielectric layer whose material definition in the *layers_<pm>.out* file matches one of the flexible dielectric material names, are assigned appropriate flex subtypes according to their base type. See “Subtypes to Support Flex/Rigid Flex Manufacturing” in the *Getting Started With ODB++Design*. Sets configuration parameter eda_flex_material.
Symbol type for lines and arcs	Sets the symbol type for lines and arcs of the step profile polygon. • **Round** — The symbol type is round. • **Square** — The symbol type is square. Sets configuration parameter eda_cadence_profile_sym_type.
Turn eda_cadence_silk_fill on	Fills surfaces on Allegro silk screen layers. Sets configuration parameter eda_cadence_silk_fill.
Turn eda_cadence_add_boundary_layers on	Controls whether to use data with CLASS = BOUNDARY in the *geom_<pm>.out* file to create boundary layers. • **Yes** — Creates a boundary layer for each line with CLASS = BOUNDARY. • **No** — Does not create boundary layers. Sets configuration parameter eda_cadence_add_boundary_layers.

Table 1-6. Specifying Configuration Parameters Page (cont.)

Object	Description

Keep auxiliary layers name as in artwork	Controls whether to translate the names of silk screen, solder paste, and solder mask layers.
	• **No** — Renames auxiliary layers based on their subclass in the *films_<pm>.out* file:
	  • "SILKSCREEN_TOP", "sst"
	  • "AUTOSILK_TOP", "sst"
	  • "SILKSCREEN_BOTTOM", "ssb"
	  • "AUTOSILK_BOTTOM", "ssb"
	  • "PASTEMASK_TOP", "spt"
	  • "PASTEMASK_BOTTOM", "spb"
	  • "SOLDERMASK_TOP", "smt"
	  • "SOLDERMASK_BOTTOM", "smb"
	• **Yes** — Keeps the auxiliary layer names as defined in the *films_<pm>.out* file.
	Sets configuration parameter eda_cadence_keep_auxiliary_layers_name.

Turn eda_cadence_thermal_error on	The translator aborts with a message listing the padstack / thermal names that did not have a match in the models file. Sets configuration parameter eda_cadence_thermal_error.
Use thermal model file	Controls whether a thermal file is used. • **Default** — Use a default model that uses direct connect and no thermals. • **Use file** — Use a model stored in a thermal model file.
Set file name of thermal model	The file to be used when Use thermal model file = Use file. Click **Select Model** to select the model in the file.
Back 	Displays Page 2 of Specifying Additional Parameters. See Table 1-5.
Next 	Runs the translation.

Chapter 2
System Administrator Notes

Information is provided that might be of interest to you as you convert a Cadance Allegro design to an ODB++ product model.

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Release Notes

Features and resolved issues are listed for versions of ODB++Design Inside for Cadence Allegro since Version 9.0.

Version 2211 Features and Resolved Issues

ID	Resolved Issue
EBS-110665	Incorrect netpoint location for feature translated from Cadence
EBS-135095	BRD2ODB Fails when installed on a server
EBS-136524	ODB++ inside export negative feature incorrectly
EBS-137857	Incorrect profile created from a single circle feature
EBS-138806	ODB2BRD Returns Undefined Symbol error on Linux

Version 11.5 Features and Resolved Issues

Switches have been added for the following additional translation parameters (EBS-129949): “Create Rout From Artwork Layer” (-ral), “Import Areas-Constraint region” (-rr), “Remove redundant dielectric” (-rrd), “Use panel outline as profile” (-up). See “Command Line Parameters” on page 69.

Context, type, and reference layer parameters are set correctly for solder mask, solder paste, and silk screen layers associated with inner copper layers. (EBS-131370). See “Support for Mask Layers Associated With Inner Copper Layers” on page 85.

The translation algorithm now recognizes filled pads in mask layers (EBS-136852). See the description of the *geoms_<pm>.out* file in “Generated Extract Files” on page 60.

ID	Resolved Issue
EBS-47753	Configuration Parameter eda_cadence_copper_layers_from_films was set to obsolete.
EBS-131060	The incorrect functioning of the feature contour fix caused some features to disappear. This is now fixed.
EBS-132198	The translation placed a mirrored component on the wrong side. The code has been fixed so that mirroring is not ignored.

Version 11.4 Update 1 Features and Resolved Issues

Additional parameter “Create Rout From Artwork Layer” specifies the layer in the Allegro artwork from which to create the rout (outline). (EBS-130054). See “Specifying Additional Parameters Pages” on page 21.

ID	Resolved Issue
EBS-128548	New format DFA table is now created on ODB++ export from Cadence Allegro. See "Cadence Allegro DFA Table" on page 83.

Version 11.4 Features and Resolved Issues

The Skill creates an additional *.out* file that contains hole type and pad usage information. (EBS-110813). See "Support for Padstack Types and Usage" on page 87.

Version 11.3 Features and Resolved Issues

The "DFA" option has been added for the "Component Outline" parameter (EBS-104780). See "Support for DFA Boundaries" on page 88.

Components marked as "BOM ignored" are excluded from the BOM and ignored in analysis actions (EBS-122260). See "Support for Components Excluded From BOM" on page 87.

Intentional shorts are read in and not reported as violations by Netlist Analyzer (EBS-111377). See "Support for Intentional Shorts" on page 87

Test point shapes are created in document layers for top and bottom (EBS-111890). See "Support for Test Point Shapes" on page 87.

ID	Resolved Issue
EBS-106873	Translation froze when handling a very complex component made up of over 3000 shapes in the EDA data. Fixed by limiting connection attempts to 3000 shapes.
EBS-109463	The rendering of the profile for a job with two sets of shapes, one of which results with the step profile and the other constructs cutouts some of which are returned as holes, was fixed by applying all holes to the profile, and, if the profile itself is included as a cutout (resulting with an empty contour after the cutouts are subtracted from the profile), using the new shape comprised of the profile and the holes as the step profile, instead of the one calculated before applying cutouts.
EBS-110090	The rendering of the outline of a single-shape package was fixed by validating the shape correctness as a post-process, and not during translation.
EBS-110898	When translating with the additional parameter Suppress Unconnected Pads = yes, the suppression of a connected pad was resolved by setting the additional parameter Fully isolated pads = yes for cases when the touching feature is a pad or when the touching line/arc is not snapped to the pad center.
EBS-111431	The issue of ODB++ and Gerber differences for SIP data was fixed by changing the simplify algorithm to have 0.25 mil as the maximum tolerance.

ID	Resolved Issue
EBS-111755	The placement of components with both sides specified in the *pinsside_<pm>.out* file was fixed by using the mirror flag.
EBS-125943	The crash caused by the contour union function returning an empty contour as a union of two non-empty contours was fixed by adding a new function to check the result and perform the union again using the old contour operation functions.

Version 11.2 Features and Resolved Issues

The translator now supports drills for which no pad is defined on any copper layer (ID = dts0101411754). The drill span is read from the DRILL_TOP_NAME and DRILL_BOTTOM_NAME fields of the pins file. If no values exist, the drill span is taken from START_LAYER_NAME!END_LAYER_NAME in the pinsside file. See "Generated Extract Files" on page 60.

Valor NPI maintains the same behavior for DFA Spacing as Cadence Allegro by reporting only those components/packages that are referenced in the DFA files (ID = dts0101404514).

ID	Resolved Issue
dts0100899561	Wirebond layer netlist information is not read from the *.aif* file.
dts0100983967	Length of .eda_layers attribute prevents the displaying of layer.

Version 11.1 Features and Resolved Issues

The translator now supports partial ODB++ output (ID = dts0101391271). See "Support for Partial ODB++Design Output" on page 88.

The translator now supports flex subtypes. (ID = dts0101299131). See "Support for Flex Subtypes" on page 88.

The translator now supports boundary layers (ID = dts0101377356). See "Support for Boundary Elements" on page 88.

The translator now support backdrill size. (ID = dts0101364515). See "Support for Backdrill Size" on page 88.

Changes in the Padflash additional parameter's Substitute option (ID = dts0101389429). See Table 1-3 on page 24.

Configuration parameter diodes_pin1_name controls the assignment of pin 1 in diodes (ID = dts0101360427). See Table 1-6 on page 33.

ID	Resolved Issue
dts0101124925	Through hole pad flagged as SMD causing erroneous "Hole in SMD" flags.
dts0101212606	Bond finger oval represented using special symbols when could have just been ovals
dts0101290601	Cadence Input v10.0 renders special symbol pad shape to standard pad shape
dts0101363294	Customer's .out files take 2-3 hours to translate in NPI
dts0101381641	When decide on Zone type we should not check dielectric layers.
dts0101383324	Impedance TraceLayer should be the layer row UID from Matrix and not the layer UIDw.
dts0101384090	Translation of .out files from ODB++ inside ver 10.2 hangs and does not complete
dts0101396404	ODB++ Inside takes many hours or doesn't complete based on Symbol Tolerance settings

Version 11.0 Features and Resolved Issues

Allegro Buildup and Core definitions can be taken from the LAYER_FUNCTION field (ID = dts0101333681). See “Support for Dielectric Layer Subtypes” on page 89.

ID	Resolved Issue
dts0101320398	False Broken Nets Appear in Netlist Analysis when there are Two Dielectric Layers above the Bottom Copper Layer
dts0101323771	Allegro EDA translation fails with error message “dml_stp-48008-Illegal profile”
dts0101329507	Cadence design with embedded components fails to translate
dts0101335455	APD
dts0101354176	Cadence translation failing
dts0101358536	CAD: While running vNPI flow from Cadence - There's a problem creating a new folder
dts0101358537	CAD: The flow is getting into “Checklist Editor” and run the analysis without checking first if the user want to do so, in Cadence flow.
dts0101359802	Error about progress bar while translation of cadence data
dts0101359840	netpoint for U-shape component is created at an inappropriate location, with no connection to copper

Version 10.1 Features and Resolved Issues

The Valor NPI attribute Hatch is assigned to lines and arcs with CROSS_HATCH_SHAPE defined in the geometry.

The translation can read embedded components from the component file, set the package according to the definition, and set the side according to EMBEDDED_STATUS.

Netlist Analyzer can handle backdrills.

ID	Resolved Issue
dts0101282557	A value of 0.005 inch (0.00127 mm) could not be entered into Symbol Tolerance parameter for ODB++ Inside.
dts0101268720	Testpoints were coming in with large bounding box with Allegro EDA translation.
dts0101280676	Pad suppression gave inconsistent results.
dts0101282681	Problem importing dielectric layers from .sip format.

Version 10.0 Features and Resolved Issues

Cadence Allegro version 17.2 is supported.

If the Cadence Allegro design contains bend areas, this information is stored in the ODB++ product model in a layer named bend_area. This is a positive board layer of type mask and subtype bend_area. Bend area information is used in rigid flex analysis.

The file *zone_<pm>.out* contains Cadence Allegro zone information. See "Generated Extract Files" on page 60.

Cadence Allegro property values can be stored in user attributes in the product model. See the following topics:

- "Importing Allegro Component Properties" on page 78
- "Importing Allegro Geometry Properties" on page 76.

The file *pinsside_<pm>.out* establishes side on which the component is placed. See "Generated Extract Files" on page 60.

The product model profile is generated from OUTLINE lines or from DESIGN_OUTLINE lines of the geoms file. See "Generated Extract Files" on page 60.

Command line parameter -noDPW suppresses automatic launching of the wizard. See "Command Line Parameters" on page 69.

Embedded passive components in a Cadence Allegro design can be translated. The value of EMBEDDED_LAYER, from the file *pins_<pm>.out*, is stored in ODB++ attribute .placement_layer. See "Generated Extract Files" on page 60.

The option to read the regions file can be specified in the additional parameters. See "Specifying Additional Parameters Pages" on page 21.

ID	Resolved Issue
dts0101067749	The translator assigned attribute Copper Text to all features outside the profile.
dts0101247467	The translator exited unexpectedly.
dts0101237609	Translation failed.
dts0101235664	A CAD file that translated correctly in an earlier version, did not translate in the current version.
dts0101251698	There was an error translating Cadence *.out* files.
dts0101254313	Cadence 17.2 Extraction was not reading profile data. The product model profile is now generated from OUTLINE lines or from DESIGN_OUTLINE lines of the geoms file.
dts0101254320	The translator did not read the tech file of Cadence 17.2 correctly.

Version 9.8 Resolved Issues

ID	Resolved Issue
dts0100731892	Data from INFO command was different from expected.
dts0100800426	Allegro Board Outline did not translate correctly.
dts0100896990	Netlist information for a wirebond layer was not translated correctly due to .aif syntax limitation.
dts0101186642	Angle traces got closer to each other after being loaded into Valor NPI.
dts0101198647	Padstack errors were reported when importing from Cadence Allegro.

Version 9.7 Features and Resolved Issues

Support was added for translation from Cadence Allegro Version 17.

Enhancements were made to the ODB++ Viewer:

- Any number of layers can be displayed.
- A Popview can be created.

- A count of highlighted features is displayed in the status bar.

ID	Resolved Issue
dts0101002856	Cadence Allegro translation did not match Gerber.
dts0101167225	Setup Mode should appear in the drop-down list of 'Action' and not in a separate check box.
dts0101169738	Input path was empty in setup window.
dts0101186168	Launching Valor NPI from Cadence Allegro started in Setup Mode.
dts0100878497	Model did not show up in the GUI, even though the Thermals selection was set to Use file.
dts0100976718	Allegro EDA interface read Component to the opposite side.
dts0101095048	The imported Allegro data was different from earlier versions.
dts0101138566	EDA input failed when the Defaults file specified an ODB Job name.
dts0101140049	Netlist analyzer reported a false alarm.
dts0101141281	Incorrect translation of profile from Cadence EDA.
dts0101164610	Any layer to Any layer backdrill data was not translated.
dts0101166558	Cadence Component translation was different from earlier versions.
dts0101168928	Support buried back drill in Cadence input.
dts0101178541	edt_chk-141005-No results were available until the action was executed.

Version 9.6 Features

You can export to ODB++ Version 8 format, as well as to ODB++ Version 7. (ID = dts0101139756)

If the Cadence Allegro design contains a DFA Table, ODB++ Inside reads the information and stores it in the ODB++ structure, if you export to ODB++ Version 8. The DFA table defines the spacing required between various types of components. This information can be used during Valor NPI Assembly Analysis when reporting to the component to component (c2c) spacing category.

Spacing values for the bottom of the board are read in from the Cadence Allegro DFA table, as well as spacing values for the top of the board. This information can be used by Valor NPI Assembly Analysis when you run a component analysis on the bottom of the board. (ID = dts0101121992)

Information from these files is stored with the product model if you export to ODB++ Version 8:

- *crosssection_<product_model>.out* — To get the impedance of the layer. To obtain this data, choose **show single impedance** () in the Layout Cross section window.
- *dfa_<product_model>.out* — Contains the DFA data () for component analysis.
- *conn_<product_model>.out* — Contains net connections.
- *regions_<product_model>.out* — Contains regions.

Version 9.5.1 Changes in Behavior

These *out* files are created, but because the translator exports to ODB++ Version 7, the data in these files is not available in this version of the translator. See "Generated Extract Files" on page 60.

- *crosssection_<product_model>.out* — To get the impedance of the layer. To obtain this data, choose **show single impedance** () in the Layout Cross section window.
- *dfa_<product_model>.out* — Contains the DFA data () for component analysis.
- *conn_<product_model>.out* — Contains net connections.
- *regions_<product_model>.out* — Contains regions.

Version 9.4 Features and Resolved Issues

Support was added for configuration parameter eda_cadence_read_dra_file. See "Configuration Parameter Settings" on page 47. (ID = dts0100855100, CCR = 984737)

Support was added for mirrored padstacks. (ID = dts0100898527, CCR = 1001474)

Support was added for user defined top and bottom component outline errors. (ID = dts0100705169)

ID	Resolved Issue
dts0100902428	Characters were missing from drill figures in backdrill drill legend translations.
dts0100902941 CCR 1029080	Pad for the rotated symbol RefDes MK4 was offset.
dts0100902951 CCR 1027161	Converting arc to line caused a mismatch between the design and the ODB++ output at layer Inner-14 (8.845 -5.118)

ID	Resolved Issue
dts0100903000 CCR 0640273	The translation was incorrect when the pad from the geometry file is a special symbol and its location is according to the symbol center.
dts0100913049 CCR 1033890	The translator combined multiple wirebond layers into a single wirebond layer in the ODB++ output.
dts0100939413	Command line switch abbreviations did not work correctly.

Version 9.3 Features and Resolved Issues

The Graphic User Interface has been enhanced.

ODB++ Viewer can read TGZ files (ID = dts100796685)

ODB++ Viewer can display Step and Repeat tables (ID - dts100805216)

ID	Resolved Issue
dts0100704940	Fixed fill surface issue.
dts0100748565	Pads with chamfered corners are included in the resulting ODB++ file.
dts0100754139	Fixed issue.
dts0100776652	Fixed error when using the translator.
dts0100791118	Components from top side do not now fall to the bottom side.
dts0100802150	Fixed component keepout issue.
dts0100829891	Suppress unconnected pads correctly handles connected pads.
dts0100857527	Extracted files from Allegro 15.5.1 can now be translated
dts0100873791	Fixed zero Mil rout width issue.
dts0100880260	Fixed issue.
dts0100898527	Added support for mirror padstacks.
dts0100902941	Fixed pad offsets.
dts0100902951	Fixed arc handling.

Version 9.2 Features and Resolved Issues

ODB++ Viewer can read TGZ files (ID = dts100796685)

ID	Resolved Issue
dts0100747607	APD 15.5.1 cannot extract the data using *valor_ext.il*.

Version 9.1 Features and Resolved Issues

Designs from Cadence Allegro V16.3 can be translated to ODB++.

The Allegro Export ODB++ dialog box has been enhanced.

You can display the resulting ODB++ file in the ODB++ Viewer.

Different AIF formats are supported. (ID = 705745)

A new cavity class is supported (ID = 744654)

ID	Resolved Issue
dts0100705391	A problem with Minimum Comp Height DFM category.
dts0100705816	Cadence Wirebonding Translation issue with Config parameter eda_cadence_copper_layers_from_films
dts0100705819	Line is missing in log after second translation.
dts0100705935	A problem with Cadence Allegro EDA Translation.
dts0100706074	ODB is inconsistent with source file (Cadence APD)
dts0100706181	A problem with Cadence Allegro EDA input.
dts0100706207	Netpoint is on cadnet.top and bot instead of tru.
dts0100706251	ODB++ Inside parameter problem when run in command line
dts0100707590	ODB++ Inside and problems with backdrilling.
dts0100712910	Area rules not rotating with part
dts0100717567	A problem with Cadence Allegro EDA input.
dts0100722970	brd2odb v8.2 does not work on linux 64 bit
dts0100725459	Only 8 decimal places accuracy when downgrading to odb++v6.0
dts0100734546	Problems with partial ODB++.
dts0100741482	Help about window.
dts0100746075	Chamfered Pads will be shown as rectangle Pad in ODB++; Export ODB++ and Import to VUV8.2 shows wrong results.
dts0100749144	ODB++ is not generating the Drill Table correctly.
dts0100756289	dofile issue - CLASS COMPONENT GEOMETRY and SUBSTRATE GEOMETRY are not displayed
dts0100757114	Generated ODB++ output file contains incorrect Thermals.
dts0100757748	Features are wrong in the translated board
dts0100759390	Problem when installing ODB++ Inside for Allegro 9.1

ID	Resolved Issue
dts0100759615	SAT - BRD2ODB ODB++ Inside 9.1 ODB++ viewer shows incorrect image of top copper layer
dts0100760727	"Fatal error occurred while exporting design" when exporting ODB++ with decal custom thermals set to 8 spokes
dts0100762522	A problem with Pad Suppression in Allegro ODBI 9.1

Version 9.0 Resolved Issues

ID	Resolved Issue
9419	There was no way to specify that component outlines should be taken from user-defined classes. See the Component Outline parameter in "Specifying Additional Parameters Pages" on page 21.
14875	Translation failed if the net properties file was very large.
16797	The COMPONENT KEEPOUT class was not recognized as defining a keepout area.
16855	The dimensions of the profile were incorrect.
16878	FILLETS from Cadence Allegro V16.2 were not assigned the .tear_drop attribute during translation.
16342, SF 8413, SF 8665	Features were missing when they were defined in a mirrored padstack. See "Support for Mirrored Padstacks" on page 97.
16900, SF 8715	Translation failed during profile creation.
SF 11342	Application crashed during translation.
SF 11541	If there are components with both ASSEMBLY_TOP and ASSEMBLY_BOTTOM, or PLACE_BOUND_TOP and PLACE_BOUND_BOTTOM, how does the translator decide on the placement side?
SF 8032	Slot figures were missing from the translation.
SF 8664	If a drill is OBLONG_Y and its size in the pins file does not match its size in the padstack, the drill slot was sometimes rotated incorrectly relative to the copper layer pads.
SF 8758	ODB++ Inside for Cadence Allegro could not be run on Linux RH5.

ODB++Design Entity Naming Rules

ODB++Design entity names must follow the naming conventions.

- The length of any name must not exceed 64 characters.

- Only these characters are legal in an ODB++Design entity name:
  - lower case letters (a - z)
  - digits (0 - 9)
  - hyphen (-), underscore (_), dot (.), plus (+)
- Names must not start with hyphen (-), dot (.), or plus (+), and must not end with a dot (.). The one exception is system attributes, which start with a dot. User attributes must not start with a dot.

Running the Translator from Design Workbench

When Allegro is to be launched from the Allegro Design Workbench, environment variable PCBDW_USER_PATH must be set when ODB++Design Inside is installed.

Procedure

1. Locate the Allegro Design Workbench launch wrapper file *adwstart.bat*. This file is typically located under the install tree.
2. Edit *adwstart.bat* to include this line:

   ```
   set PCBDW_USER_PATH=<path to ODB++Design Inside>\nv\bin
   ```

   where <*path to ODB++Design Inside*> is the path to the ODB++Design Inside module, typically *C:\MentorGraphics\Allegro Export ODB++Design*.

Configuration Parameter Settings

Configuration parameters are defined in the file *config* that is installed with Allegro Export ODB++Design, in $ALLEGRO_BRD2ODB (the same directory as the program executables).

If you run ODB++Design Inside for Cadence Allegro from a line mode command, you can specify a different location for the *config* file, in parameter -cfg. See "Command Line Parameters" on page 69.

The *config* file can contain parameters used by several translators.

Lines of the *config* file have format <*parameter_name*>=<*parameter value*>.

Note

Edit the file to set the appropriate values for the configuration parameters, before opening the translator. If you edit the *config* file after opening the translator, the new values are not used.

There are general configuration parameters and configuration parameters that are specific to the Cadence Allegro translation.

General Configuration Parameters

General Configuration Parameter	Type	Default	Description
drc_comp_height	Text	drc_comp	Document layer containing component height restriction areas (used to check for components above or below height limits in height restricted areas).
attr_value_correct			Controls how the translator handles illegal attribute values (out of range, etc.) that are input with a design. • **Yes** — The attribute is reset to its default value, and a message is written to the log. • **No** — Translation is halted.
drc_comp_keepin	Text	drc_comp	Document layer containing component keepin areas (to check for components outside keepin areas).
drc_comp_keepout	Text	drc_comp	Document layer containing component keepout areas (to check for components inside keepout areas).
drc_pad_keepout	Text	drc_route	Document layer containing pad keepout areas (to check for pads inside keepout areas).
drc_plane_keepout	Text	drc_route	Document layer containing plane keepout areas (to check for planes inside keepout areas).
drc_route_keepin	Text	drc_route	Document layer containing rout keepin areas (to check for traces, planes, pads, vias outside the keepin areas).
drc_route_keepout	Text	drc_route	Document layer containing rout keepout areas (to check for traces, planes, pads, trace-bends inside keepout areas).
drc_tp_keepin	Text	drc_tp	Document layer containing testpoint keepin areas (to check for testpoints outside keepin areas).
drc_tp_keepout	Text	drc_tp	Document layer containing testpoint keepout areas (to check for testpoints inside keepout areas).

General Configuration Parameter	Type	Default	Description
drc_trace_keepout	Text	drc_route	Document layer containing trace keepout areas (to check for traces inside keepout areas).
drc_via_keepout	Text	drc_route	Document layer containing via keepout areas (to check for vias inside keepout areas).
eda_flex_material	Text		The name(s) of flexible dielectric materials. Multiple values are separated by semicolons (;). For example: POLYIMIDE;POLYIMIDE_FILM At import of Cadence Allegro data, the copper layers below and above a dielectric layer whose material definition in the *layers_<pm>.out* file matches one of the flexible dielectric material names, are assigned appropriate flex subtypes according to their base type. See "Subtypes to Support Flex/Rigid Flex Manufacturing" in *Getting Started With ODB++Design*.
gns_pdf_viewing_prog	Text		Default program path and arguments to open a PDF file. Used for standalone translators only.

Cadence Allegro Specific Configuration Parameters

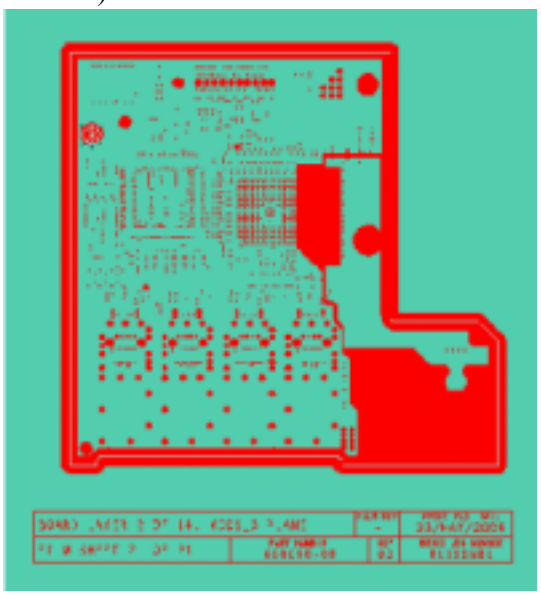
Configuration Parameter	Type	Default	Description
eda_cadence_add_nets_from_geometry	Boolean	yes	Controls whether net information is read from the connectivity out file or from the geometry out file. **Yes** — Work as before and take net information from the geometry file *geoms_<pm>.out*. (Default) **No** — Take net information from the connectivity file *conn_<pm>.out*.
eda_cadence_apd_bot_name	Text	base	The name used to indicate the bottom layer in APD files. When Cadence APD files are translated, the default name for the bottom layer is base. If you have APD files that use a layer name other than base for the bottom layer, you can specify an alternate name.

Configuration Parameter	Type	Default	Description
eda_cadence_apd_top_name	Text	surface	The name used to indicate the top layer in APD files. When Cadence APD files are translated, the default name for the top layer is surface. If you have APD files that use a layer name other than surface for the top layer, you can specify an alternate name.
eda_cadence_check_package_shape	Boolean	No	If a design is likely to have components with identical package names but different geometries, you can have the translator check the geometry of a component if its package name is identical to that of another component. • **Yes** — If a component has the same package name as another component, the package shapes in the file *comps_<product_model>.out* are compared. If they are not the same, a new package is created for the second component. The new name is created by adding a suffix consisting of a plus sign (+) and an index number. • **No** (default) — If a component has the same package name as another component, they are assumed to have the same geometry. No checking is performed.
eda_cadence_delete_sort_pins_file	Boolean	no	**Yes** — Always delete temporary sort pins file. When a translation has warnings about the pins file, it does not delete the temporary pins file, so that the user can view the warnings. When running from a script, the temporary files accumulate. This parameter lets you specify that the files be deleted even if there are warnings.
eda_cadence_font_file_name	Text	ansi (the supplied font file)	The name of the font file to be used. The file must reside in $GENESIS_EDIR/all/eda/cadence/fonts. You can provide an alternate font file so that fonts used in ODB++ match the fonts used in Cadence Allegro.

Configuration Parameter	Type	Default	Description

eda_cadence_keep_auxiliary_layers_name	Boolean	No	Controls whether to translate the names of silk screen, solder paste, and solder mask layers.
			• **No** — Renames auxiliary layers based on their subclass in the *films_<pm>.out* file:
			  • "SILKSCREEN_TOP", "sst"
			  • "AUTOSILK_TOP", "sst"
			  • "SILKSCREEN_BOTTOM", "ssb"
			  • "AUTOSILK_BOTTOM", "ssb"
			  • "PASTEMASK_TOP", "spt"
			  • "PASTEMASK_BOTTOM", "spb"
			  • "SOLDERMASK_TOP", "smt"
			  • "SOLDERMASK_BOTTOM", "smb"
			• **Yes** — Keeps the auxiliary layer names as defined in the *films_<pm>.out* file.

eda_cadence_layer_polarity_source	Text	f (film)	Informs the translator to use the suppress shape fill information from the *films_xxx.out* file or from the *layers._xxx.out* file. • **f** — films • **l** — layers (Cadence Allegro only)

Configuration Parameter	Type	Default	Description
eda_cadence_pos_anti_etch	Boolean	no	Controls whether ANTI ETCH surfaces will be negative or positive. • **Yes** — ANTI ETCH surfaces will always be positive. (If the product model has a photoplot outline - positive surface - that covers legend text, the text will not be visible.)  • **No** (default) — ANTI ETCH surfaces will be negative. 

Configuration Parameter	Type	Default	Description
eda_cadence_profile_sym_type	Text	r (round)	Defines symbol type for arcs and lines of step profile polygon. • **r** — round symbol • **s** — square symbol
eda_cadence_read_dra_file	Boolean	No	Controls translation of DRA files. • **Yes** — translate DRA files • **No** — do not translate DRA files
eda_cadence_silk_fill	Boolean	No	Fills surfaces on Cadence Allegro silkscreen layers. • **Yes** — draws surfaces. • **No** — draws surfaces as outlines.
eda_cadence_sort_pins_file	Boolean	Yes	Controls whether to sort the pins file before reading it. • **Yes** — sorts the pins file alphabetically before it is read. • **No** — does not sort the pins file.
eda_cadence_sort_pins_numeric	Text	No	Controls how to sort pins. • **Yes** — sorts the pins file numerically. • **No** — sorts the pins file textually. • **yes_num_last** (or any string other than yes or no) sorts the pins file numerically but with numeric pins after pins beginning with a letter.
eda_cadence_sqa_area_layer_name	String	SQA_areas	Defines the layer where an sqa area is saved during translation from Cadence. If not defined, default value sqa_areas are saved.
eda_cadence_support_exceptional_pins	Boolean	Yes	To control whether to add to the **comps_XXX.out** file pins lacking names and component designation, or whose components do not appear in the file. • **Yes** — (default) Adds a component named no_refdes+XX. • **No** — Ignore the pins.

Configuration Parameter	Type	Default	Description
eda_cadence_suppress	Boolean	No	Default value for option Suppress Unconnected Pads. • **Yes** — Perform unconnected pad suppression. • **No** — Do not suppress unconnected pads.
eda_cadence_suppress_shape_fill_setting (obsolete)	Text	f	Obsolete - replaced by the Suppress shape fill option of the Cadence Matrix File Editor.
eda_cadence_therm_err	Boolean	No	• **Yes** — The translation process will abort with a message listing the padstack / thermal names that did not have a match in the models file. (Thermals Mode in Input Parameters must be set to Use File for this configuration parameter to work). • **No** — Does not flag missing thermals.
eda_cadence_v14_popup (obsolete)	Boolean	Yes	Obsolete.

Setting Environment Variables

These environment variables are used to define values used by the translator.

Environment Variable	Default	Mandatory	Explanation
BRD2ODB_TMP	None	Yes — for Windows XP No — otherwise	Location for storing temporary files. If not defined, the translator stores files in the location defined by environment variable APPDATA\translator_logs.

Thermal Model Configuration

Cadence Allegro Designer (Version 13) does not explicitly define the shape of the thermal pads or the Padflash definitions. Typically, these definitions are deferred until the Gerber wheel apertures are defined. However, to generate accurate board data, ODB++Design Inside for Cadence Allegro requires the use of a Thermal Model to explicitly define these shapes.

Structure of the Thermal Model File **55**
Thermal Model Examples **58**

Structure of the Thermal Model File

The thermal model file contains a units statement and one or more model definitions. Each model describes one type of behavior. The file can be built in such a way that each model is customized for a specific customer, a product type, or an EDA system.

See "Thermal Model Examples" on page 58.

This is the structure of the file:

```
.units [inch|mm]
.model <name>
... model info ....
.model <name>
... model info ....
.model <name>
... model info ....
```

Lines starting with the number sign (#) are comments and are ignored.

Units Statement

The units directive must be the first line in the file.

```
.units [inch|mm]
```

It specifies the measurement units that will be used for the models.

- **inch** — 0.001 inch (mil) units.
- **mm** — 0.001 mm (micron) units.

Model Statement

Each model definition begins with the model directive.

```
.model <name>
```

The name is limited to 64 characters that can include letters, digits, and these characters: dash (-), underscore (_), period (.), plus (+).

Rule Statements

Each model definition consists of the model directive followed by a set of rules expressed in Backus-Naur Form (BNF). The rules are used for substitution of clearances to thermal pads. In the EDA system, a padstack or padflash always defines the shape of the clearance in the Power & Ground layer. It is the electrical net of the pin that determines whether the clearance will be retained or will be substituted by a thermal pad.

When the translator processes the data, it determines whether a particular clearance must be converted to a thermal relief pad. It is at this point that the model, with the name provided as a translation parameter, is consulted.

Each rule consists of a condition and a derivation.

<rule> ::= *<condition>* : *<derivation>*

If the condition is met, then the thermal shape described in the derivation is used for the pad. The first match is used.

Condition

The condition of a rule consists of the type of padstack or the name of the padstack, optionally followed by equations defining the clearance size or drill size that match the rule.

<condition> ::= *<type>* {*<equation>*}

Type

<type> ::= PIN | VIA | *<geometry_name>* | '*<geometry_name>*'

- PIN or VIA — Keyword indicating the type of padstack that matches the rule.
- *<geometry_name>* — Name of the padstack that matches the rule. This is the name of the padstack geometry used in the EDA system. For Cadence Allegro, the padflash definition is used.

  This name can be surrounded by quotation marks, accommodating the rare case of a padstack called PIN or VIA.

A model can contain some rules defined with PIN or VIA types and some rules defined with *<geometry_name>*.

Equation

<equation> ::= [D|C] ['<' | '<=' | '=' | '>' | '>='] *<value>*

The equations represent numerical checks for the drill size (D) or clearance size (C) with which the padstack is to be compared. These are some examples:

PIN C>80 — This matches pin padstacks with clearances greater than 80 units.

VIA C<=40 D<=12 — This matches via padstacks with clearances less than or equal to 40 units and drill less than or equal to 12 units.

Derivation

The rule derivation specifies the shape to be used. It can be a standard symbol or it can be based on the clearance and drill size and shapes.

<*derivation*>::= NULL | '<*sym_name*>' | <*set_values*>

NULL

The NULL keyword can be used to create direct connect. The clearance will be deleted completely without a thermal pad.

Symbol Name

The symbol name can be any legal ODB++ standard name, semi-standard name, or special symbol (such as 003, thr80x50x0x4x10).

<*sym_name*>::= Standard, semi-standard, or special symbol.

Set Values

If a standard symbol name does not provide enough flexibility, the derivation can be defined based on the clearance and drill size and shapes.

<*set_values*> ::= <*od*> <*id*> <*tie*> <*num_ties*> <*angle*> <*oshape*> <*ishape*> <*style*>

- <*od*> ::= [C+value | C-value | D+value | D-value | value]

  The outer diameter can be specified as a fixed value or as a value added or subtracted from the Clearance (C) or Drill (D) sizes.

- <*id*> ::= [C+value | C-value | D+value | D-value | value]

  The inner diameter can be specified as a fixed value or as a value added or subtracted from the Clearance (C) or Drill (D) sizes.

- <*tie*> ::= <*value*>

  The size of the tie.

- <*num_ties*> ::= <*value*>

  The number of ties.

- <*angle*> ::= <*value*>

The start angle for the first tie in degrees.

- <*oshape*> ::= R | S | C

  The shape of the outer ring can be round (R), square (S), or the same shape as the clearance (C).

- <*ishape*> ::= R | S | C

  The shape of the inner ring can be round (R), square (S), or the same shape as the clearance (C).

- <*style*> ::= R | S

  The style of the thermal near the tie can be rounded (R) or squared (S).

Thermal Model Examples

These examples show a thermal model file with two models, a thermal model file using Cadence Allegro padflashes, and an example of a typical derivation statement.

Thermal Model File With Two Models

```
.units inch
#
.model std
# All via clearances with drill size less than 40 mils to be cleared.
# Other vias will have a thermal that is a function of the drill size.
#
VIA D>=40  : D+40 D+20 10 4 0 R   R   S
VIA        : NULL
#
# All pin clearances with clearance size less than 45 mils to be cleared.
# Other clearances will have a thermal that is a function of the
# clearance size, in two groups - Clearances equal to and above 165 mils,
# and clearances equal to or above 45 mils.
#
PIN C>=165 : C    C-30 15 4 0 C   C   S
PIN C>=45  : C    C-20 10 4 0 C   C   S
PIN        : NULL
#
.model symbols
#
# This model matches specific padstack names with fixed thermals. This is
# useful when the EDA system used a limited set of fixed names
#
D73: 'ths85x65x45x4x12'
D74: 'ths62x42x45x4x12'
D75: 'ths100x80x45x4x12'
D76: 'ths120x100x45x4x12'
D77: 'ths160x140x45x4x12'
```

Thermal Model File Using Cadence Allegro Padflashes

```
.units inch
.model allegro_model
# Direct replacement of symbols
# Replace the padflash named "TH05" with a round clearance of 5 mils.
TH05: 'r5'
# Replace the padflash named "T165X145X20X45" with a square thermal with
# an outer diameter of 165 mils, inner diameter of 145 mils
# with four ties each of 20 mils, first starting at 45 degrees.
T165X145X20X45: 'ths165x145x45x4x20'
# Replace the padflash named "5MIL" with a direct connection
5MIL: 'null'
# calculated values
# Place a direct connect for all VIA pads
VIA: NULL
# For pins with a clearance less than or equal to 45 mils,
# place a rounded thermal with outer diameter the size of the
# clearance inner diameter 20 mils smaller, 4 ties of 20 mil
# starting at 45 degrees outer and inner diameters shaped as
# the clearance
PIN C<=45 : C   C-20 15 4 45 C C R
```

Typical Derivation Example

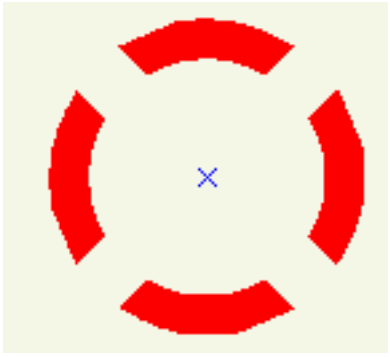
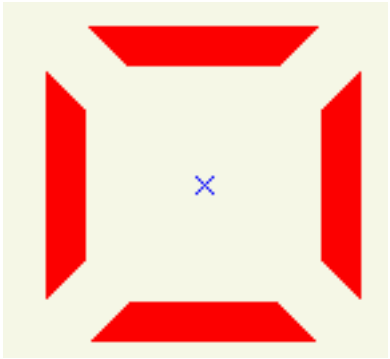
This is an example of typical derivations:

```
C   C-20 15 4 45 C   C   S
```

The example specifies these values:

Parameter	Value	Description
od	C	The outer diameter is the same as the clearance.
id	C-20	The inner diameter is 20 units less than the clearance.
tie num_ties	15 4	There are 4 ties, 15 units each.
angle	45	Starting at 45 degrees.
oshape ishape	C C	Both rings are the same shape as the clearance.
style	S	The style is squared.

This specification will produce different thermals depending on the padstack:

Padstack	Symbol	Graphic
Padstack with round 80 mils clearance.	ths80x60x45x4x15	
Padstack with square 80 mils clearance.	s_ths80x60x45x4x15.	

Generated Extract Files

These files, created by Cadence Allegro, contain information about the design.

If you are running ODB++Design Inside from within Cadence Allegro, you can specify a *.brd* file as the input path. If you are running ODB++Design Inside stand-alone, you must specify a directory containing the *.out* files that have been extracted from Cadence Allegro.

The extraction files are generated using *$ALLEGRO_BRD2ODB/valor_ext.il* skill code.

The variable <*pm*> in the file names represents the name of the current product model.

For CAD layers to be present in the generated ODB++, you must create the films for those layers.

File	Description

comps_<pm>.out	The components file contains the outline shape of all the components.
	The outline records are typically in subclass PLACE_BOUND_<*side*> but may also be in subclass ASSEMBLY_<*side*> or DFA_BOUND_<*side*>.
	This is a typical component in the comps file:
	`S!PLACE_BOUND_TOP!3544 1 0!`
	`.....J0508!CON60X2!!CON60X2!1100.00!675.00!90.000!NO!`
	`.....LINE!1400.00!325.00!1400.00!4075.00!0.00!!!!!SHAPE!`
	`S!PLACE_BOUND_TOP!3544 2 0!`
	`.....J0508!CON60X2!!CON60X2!1100.00!675.00!90.000!NO!`
	`.....LINE!1400.00!4075.00!700.00!4075.00!0.00!!!!!SHAPE!`
	`S!PLACE_BOUND_TOP!3544 3 0!`
	`.....J0508!CON60X2!!CON60X2!1100.00!675.00!90.000!NO!`
	`.....LINE!700.00!4075.00!700.00!325.00!0.00!!!!!SHAPE!`
	`S!PLACE_BOUND_TOP!3544 4 0!`
	`.....J0508!CON60X2!!CON60X2!1100.00!675.00!90.000!NO!`
	`.....LINE!700.00!325.00!1400.00!325.00!0.00!!!!!SHAPE!`
	These lines define the component J0508 which is based on the package CON60X2. The component is at (1.1,0.675), rotated by 90 degrees.
	The lines represent the (transformed) outline of this component.
	Component height information is read from the PACKAGE_HEIGHT_MAX field.
	Components with BOM_IGNORE data are assigned attributes “Not Populated per BOM” (.no_pop) and “Ignore Graphically/Output” (.comp_ignore).

conn_<pm>.out	The connectivity file contains net connections. Net information can be read from this file or from the geometry file, depending on the setting of configuration parameter eda_cadence_add_nets_from_geometry: **eda_cadence_add_nets_from_geometry = Yes** — Work as before and get net information from the geometry file *geoms_<pm>.out*. (Default) **eda_cadence_add_nets_from_geometry = No** — Get net information from connectivity file.
crosssection_<pm>.out	The cross section file contains the impedance of the layer. To obtain this data, choose **show single impedance** () in the Layout Cross section window of Cadence Allegro.
dfa_<pm>.out	For designs containing the old version of the DFA Spacing Table, this file stores the spacing requirements for various types of components. This information can be used during assembly analysis. See “Cadence Allegro DFA Table” on page 83

File	Description

films_<pm>.out	The films file contains the artwork information from Allegro.
	This information describes the pieces of film to be output as artwork. Each piece of film is linked to an arbitrary number of subclasses and several parameters necessary to generate the correct physical layers.
	Typical films in the file are in this way:
	`S!PIN!U0205!9!055C035!TOP!BOTTOM!EC_PRDB6!4925.00!`
	`1050.00!!!4925.00!1050.00!`
	`...PLATED!A!NULL!75.00!75.00!0.000!CIRCLE!4925.00!`
	`1050.00!90.00!90.00!`
	`S!VIA CLASS!!!VIA!TOP!BOTTOM!GND!!!4800.00!-`
	`100.00!4800.00!-100.00!`
	`...PLATED!!CROSS!50.00!50.00!0.000!CIRCLE!4800.00!-`
	`100.00!54.00!54.00!`
	Each line includes information about the film, and the location of the film. Pin lines contain component and pin number as well.
	Based on these lines, toeprints are added to components and drill holes are added to the appropriate drill layers.
	Lines with CLASS = BOARD GEOMETRY or EMBEDDED GEOMETRY, and the SUBCLASS value consisting of two parts separated by an underscore (“_”) are used to create solder mask, solder paste, and silk screen layers. The layer name is derived from the FILM_NAME field and its type is taken from the first part of the SUBCLASS field. The second part of the SUBCLASS field provides the name of the reference copper layer. As an example, the following line would be processed by creating an ODB++ layer named inner_2_soldermask with Type = solder_mask and Reference = isl2:
	`S!inner_2_soldermask!EMBEDDED GEOMETRY!SOLDERMASK_ISL2!`
	`0!0.0000!0.0000!0.0100!0.2540!positive!no!no!no!yes!yes!`
	`no!yes!`
	Because an empty films file causes the translation to fail, the *valor_ext.il* import script checks whether the films file is empty and prompts you to check the artworks file and extract again.

File	Description

geoms_<pm>.out	The geometry file contains graphical data describing feature placement.
	It is the largest file extracted.
	Each line of the file contains graphic data that describes the feature. The file also contains the class and subclass that can be mapped to the physical layer to which the feature is added.
	The rout layer is created from the DESIGN_OUTLINE/OUTLINE data in the geometry file. The data describing features NCROUT_PATH, NCROUT_PLATED and OUTLINE is handled in this way:
	• NCROUT_PATH — Features are added to a rout layer named rout.
	• NCROUT_PLATED — Features are added to a rout layer named rout. These features receive the attribute .rout_plated.
	• OUTLINE — Features are added to a rout layer named outline if the additional parameter “Create Rout From Artwork Layer” is not set with valid data.
	This is a typical line in the file. This line adds a 6-mil line between (2.000,0.625) and (1.95,0.575) to a signal layer (SIG_2). The net of the line is CPUD9:
	`S!ETCH!SIG_2!7550 1!!!!CPUD9!!!!!!`
	`...LINE!2000.00!625.00!1950.00!575.00!6.00!!!!!CONNECT!`
	Several lines are used to describe a polygon. These four lines represent a closed shape that is translated into one surface:
	`S!ETCH!GND!2261 1 0!!!!N_GND!!!!!!`
	`... LINE!8450.00!3250.00!8450.00!4650.00!0.00!!!!!SHAPE!`
	`S!ETCH!GND!2261 2 0!!!!N_GND!!!!!!`
	`... LINE!8450.00!4650.00!12350.00!4650.00!0.00!!!!!SHAPE!`
	`S!ETCH!GND!2261 3 0!!!!N_GND!!!!!!`
	`...LINE!12350.00!4650.00!12350.00!3250.00!0.00!!!!!SHAPE!`
	`S!ETCH!GND!2261 4 0!!!!N_GND!!!!!!`
	`...LINE!12350.00!3250.00!8450.00!3250.00!0.00!!!!!SHAPE!`

File	Description
geoms_<pm>.out (cont.)	The fields NET_PHYSICAL_TYPE and NET_SPACING_TYPE correspond to attributes of the same name. The step profile is generated from lines with SUBCLASS = PANEL/ PANEL_OUTLINE, DESIGN_OUTLINE, or OUTLINE, according to the setting of parameter Use Panel Outline, using the following order: • If Use Panel Outline = Yes: a. PANEL/PANEL_OUTLINE b. DESIGN_OUTLINE c. OUTLINE • If Use Panel Outline = No: a. DESIGN_OUTLINE b. OUTLINE Data with SUBCLASS = CAVITY provides the layer profile. If no CAVITY exists, the step profile is used to define the layer profile. Data with SUBCLASS = CAVITY and GRAPHIC_DATA_10 = VOID is a layer profile hole.If configuration parameter eda_cadence_add_boundary_layer = yes, a documentation layer named boundary_<*layer_name*> is created from each line with CLASS = BOUNDARY: `S!BOUNDARY!L3!14442 1 0!!!!!!!!!!LINE!495.5!1516.5!495.5! 1651.0!0.0!!!!!SHAPE!!!!!!!!!!!!` Based on the above line, the layer boundary_l3 is created to which features are added as specified. The shorted nets information for SMD pads is taken from the NET_SHORT field. A rectangle shape with CLASS = EMBEDDED GEOMETRY, SUBCLASS = SOLDERMASK_* or PASTEMASK_*, and GRAPHIC_DATA_10 = POLYGON is used to create a filled rectangular shape in the layer specified. You can specify additional subclasses to be imported either as component properties or as user-defined attributes. See the following topics: To translate additional data stored in the geometry file, see the following tasks: • “Importing Allegro Component Properties” on page 78 • “Importing Allegro Geometry Properties” on page 76

File	Description

layers_<pm>.out	The layers file describes the order of the physical layers in the design.
	The list includes the dielectric layers and the electric layers, but it does not include such layers as solder mask and silk screen.
	This is a typical line in the layers file:
	`S!5!SIG_1!POSITIVE!!YES!!595900 mho/cm!COPPER!NO!`
	`3.98 w/cm-degC!1.2 mil!`
	The system uses fields 2, 3, 4, and 12 which provide the relative order (5), name (SIG_1), polarity (POSITIVE), and layer dielectric thickness of the layer (1.2 mil).
	If a board is described, the system also relates to the board thickness. In this example of such a string (usually located at the beginning of the file) board thickness is 26.4 mil.
	`J!D:\home\allegro\hitachi.brd!Tue Oct 15 14:53:39`
	`2014!-100.000!-100.000!1100.000!800.000!0.001!`
	`millimeters!!26.4 mil!22!OUT OF DATE!`
	The copper layers below and above the dielectric layer whose LAYER_MATERIAL definition matches one of the values of the configuration parameter eda_flex_material, are assigned the appropriate flex subtypes. See "Subtypes to Support Flex/Rigid Flex Manufacturing" in the *Getting Started With ODB++Design*.

nets_<pm>.out	The nets file contains information about net classes and properties. This file is optional. • **Classes** — Allegro declares three types of class: spacing, physical, and electrical. Every net may connect or have any combination of triplet of spacing, physical, and electrical classes, if any. The classes are defined in the technology file. • **Properties** — The file contains net properties, such as impedance. A net with property NO_TEST = Yes will have attribute testpoint_count = 0.

pads_<pm>.out	The pads file contains information about the padstacks used in the product model.
	Padstack information is required to derive the drill size at any given pin or via. It is also necessary to know which thermal is required when the pin or via has the same net as the containing surface.
	This is a typical line in the pads file:
	`S!C55N067!00014!~DRILL!o!!67.00!`
	`125.00!125.00!0.00!0.00!CIRCLE!N!J!....`
	This line specifies that padstack C55N067 has a 67 mil drill at the center (0,0) of the padstack.

File	Description
padstacks_<pm>.out	The padstacks file contains additional padstack information. Each line of the file specifies the padstack. The value in the Usage field is stored in the appropriate Valor NPI attribute: • DIE_PAD — .bump_pad • MOUNTING_HOLE — .mount_hole • BOND_FINGER — .pad_usage=bond_finger • FIDUCIAL — .pad_usage=g_fidutial • TOOLING_HOLE — .pad_usage=tooling_hole, .tooling_hole (each used by different analysis actions) Features with the value of LASER in the drillNonStandard field receive the attribute .via_type=laser.

File	Description

pins_<pm>.out	The pins file contains information about pins (toeprints) and vias.
	Each line contains information about the padstack, net, drill figure, and character added to the legend document. It also includes the location of the pin or via. Pin lines contain component and pin number as well.
	`S!PIN!U0205!9!055C035!TOP!BOTTOM!EC_PRDB6!4925.00!`
	`1050.00!!!4925.00!1050.00!`
	`...PLATED!A!NULL!75.00!75.00!0.000!CIRCLE!4925.00!`
	`1050.00!90.00!90.00!`
	`S!VIA CLASS!!!VIA!TOP!BOTTOM!GND!!!4800.00!-`
	`100.00!4800.00!-100.00!`
	`...PLATED!!CROSS!50.00!50.00!0.000!CIRCLE!4800.00!-`
	`100.00!54.00!54.00!`
	Based on these lines, Valor NPI can add toeprints to components and add drill holes to the appropriate drill layers.
	This additional information is included:
	• Information on slots — Supports functionality added in V15.2.
	• DRILL_HOLE_POSTOL and DRILL_HOLE_NEGTOL — Maximum and minimum drill tolerance values support drill tolerances added in V.15.2.
	• DRILL_ARRAY_LOCATION — Supports the Multiple/Plural Drill function added in V14.1.
	• BACKDRILL_BOTTOM_FROM, BACKDRILL_BOTTOM_LAYER, BACKDRILL_TOP_FROM, BACKDRILL_TOP_LAYER — Start layer number from the bottom or top of the design and the ending layer number from the bottom or top of the design (cut layer). The backdrill span is created from BACKDRILL_TOP_FROM to BACKDRILL_TOP_LAYER or from BACKDRILL_BOTTOM_LAYER to BACKDRILL_BOTTOM_FROM.
	• EMBEDDED_LAYER and EMBEDDED_STATUS — The value of EMBEDDED_LAYER is stored in NPI attribute .placement_layer. EMBEDDED_STATUS = BODY_UP (top) or BODY_DOWN (bottom).
	• BACKDRILL_SIZE — If no value exists, the drill padstack definition is the backdrill size.
	• DRILL_TOP_NAME!DRILL_BOTTOM_NAME — These fields provide the drill span. If no values exist, the drill span is taken from START_LAYER_NAME!END_LAYER_NAME in the pinsside file.

File	Description
pins_<pm>.out (cont.)	If pins in the pins file refer to a component not found in *comps_<pm>.out*, the translator performs one of these actions: • If an existing package name is found, the value in COMP_PACKAGE in the pins file is used as the package name. • If a package is not found, a bounding box around the pins is regarded as the outline of the package. The value in COMP_PACKAGE in the pins file is used as the package name. • If the reference in the pins file has no package, the pins are ignored. The NET_SHORT field contains intentional short data for pins and vias. The value is a colon (:) separated list of shorted nets. If a pin or via location is also a test point location, the TEST_POINT field contains a value of TOP or BOTTOM to reference the documentation layer on which the test point shape is placed. The blank field indicates that the location is not a test point. The PROBE_FIGURE field defines the test point shape as TRIANGLE, SQUARE, HEXAGON X, HEXAGON Y, OCTAGON, DIAMOND, OBLONG X, OBLONG Y, or RECTANGLE. If the value is "RECTANGE" or contains "X" or "Y", the fields GHAPHIC_DATA_3 and GHAPHIC_DATA_4 contain the width and height of the shape. Otherwise, the upper boundary for drawing the shape is determined by adding half of the smaller in width or height (GHAPHIC_DATA_3 and GHAPHIC_DATA_4) to the Y location (GHAPHIC_DATA_2).

pinsside_<pm>.out	The pinsside file is used to establish the side on which the component is placed. This is the syntax of a line of the file:
	`A!CLASS!REFDES!START_LAYER_NAME!END_LAYER_NAME!`
	`SYM_MIRROR!EMBEDDED_STATUS!`
	If the component is an embedded component, the component side is taken from the value of EMBEDDED_STATUS. BODY_UP indicates top, and BODY_DOWN indicates bottom.
	If all pins are thru-hole, the component side is determined by the values of START_LAYER_NAME and END_LAYER_NAME, and the SYM_MIRROR flag is checked.
	If there is even one SMT pin, the layer on which it is located determines the side.
	If the START_LAYER is not the top or bottom layer, but if it is the top or bottom layer of any zone, the start layer is treated as an outer layer.

props_<pm>.out	The properties file contains additional component property information. This file is optional. This allows users to read additional component properties directly into ODB++. Users requiring the extraction of additional properties can add them manually to the view file.

File	Description
regions_<pm>.out	The regions file contains information about regions.
tech_<pm>.out	The technology file is an ASCII file containing Allegro or APD parameter and constraint data. This file is optional. You can use this file to apply a uniform set of design rules and constraints to multiple designs: • User Units • Drawing Parameters • Layout Cross Section Parameters • Spacing Constraints (including clearance rules) • Net Type Clearances (to extend the scope of Signal Quality Analysis) • Physical Constraints • Electrical Constraints • User Property Definitions From Cadence Allegro version 16.0, tech files are generated in XML format. ODB++Design Inside can read either format. When the new version of the DFA Spacing Table is used, the technology file stores the spacing requirements for various types of components. This information can be used during assembly analysis. See "Cadence Allegro DFA Table" on page 83
zone_<pm>.out	The zone file contains Cadence Allegro zone information. Contours are taken from the geoms file, from the sub class ZONE_OUTLINE, according to the zone name in the geoms file. The translation creates mask layers named rigid_area and flex_area of subtypes rigid_area and flex_area, respectively. • The flex_area layer contains zones spanning only copper layers of subtype = signal_flex. • The rigid_area layers contains zones whose span includes at least one layer of subtype ≠ signal_flex. The signal_flex subtype is assigned automatically if the values of configuration parameter eda_flex_material match the dielectric LAYER_MATERIAL definitions in the layers file.

Command Line Parameters

You can run ODB++Design Inside for Cadence Allegro from the command line.

Syntax of Command Line Parameters

Usage: brd2odb [parameters]

Parameters are preceded by a dash. Some parameters accept values. Parameters must be separated by spaces. An unrecognized parameter is ignored.

If you are working in console mode (the -gui switch has not been set), missing or incorrect parameters cause the program to terminate.

ODB++Design Inside Without the User Interface

To run the translator without displaying the user interface, provide these parameters:

- -ijp <*full path to input brd files*>
- -jp <*output path*>
- -jn <*output product model name*>

For example:

```
brd2odb   -ijp  C:\inputs\allegro\design_1   -jp  C:\my_odbs   -
jn  allegro_1
```

If any of these parameters are not provided, the GUI will open even if the -gui option has not been provided.

List of Command Line Parameters

For some command line parameters there is an equivalent GUI parameter indicated in the column Equivalent GUI Parameter. The GUI parameters are described in these sections:

- "Specifying File Options and Output Options Page" on page 15
- "Specifying Partial Export Parameters Page" on page 19
- "Specifying Additional Parameters Pages" on page 21

These are the command line parameters for ODB++Design Inside for Cadence Allegro:

Parameter	Equivalent GUI Parameter	Description
-a2l -append2log		Appends log messages to existing log file *log_brd2odb*. By default, the new log file overwrites any existing log file for each translation.
-bb	Don't suppress pads on top/ bottom	Pads on top/bottom edge of blind/buried drills are not suppressed. Active only if -sp is set.

Parameter	Equivalent GUI Parameter	Description
-c <*outline*> -component <*outline*>	Component Outline	Controls which geometries are used for the component outline. • **p[lacebound]** — (default and recommended) The bounding box. • **a[ssembly]** — The limits of the assembly features. • **d[fa]** — The DFA boundary. • **u[ser_defined]**<*top*> <*bottom*> — User defined.
-cfg [<*config file*>]		Read configuration file. If <*config file*> is not specified, the default name is *$ALLEGRO_BRD2ODB/config*. The configuration file used by the translator can only be changed by using a line mode command. The configuration file must be in the same directory as the program executables.
-d -delete	Delete Extracted Files	Source extract files are deleted. By default, all intermediary files are saved. If the -gz (zip) parameter is used, the extract files are compressed.
-fi	Fully isolated pads	Only fully isolated pads are suppressed. Active only if -sp is set. Without this switch, pads are considered to be isolated in these cases: • a single totally isolated pad • two pads touching or intersecting • a pad transversed by a trace not through its center • a pad touching a surface where its center is not inside the surface
-gui		Starts the GUI version of the translator. To run the translator without displaying the user interface, provide these parameters: • -ijp <*full path to input brd files*> • -jp <*output path*> • -jn <*output product model name*> If any of these parameters are not provided, the GUI will open even if the -gui option has not been provided.
-gz -gzip	Create Archive	Compress the ODB++ folder structure of the product model to create a single *tgz* file.
-help		Lists the help switches in the console window.

Parameter	Equivalent GUI Parameter	Description
-hg -help_gui		Displays online help.
-iff	Ignore FIXFLAG	Suppression ignores the Allegro FIXFLAG setting. Active only if -sp is set.
-ijp <*path*>	Input Path	The full path to the input brd files. Default = the current working directory. This parameter is required if you want to run the translator without displaying the user interface.
-jn <*product_model*>	Output product model name	Output ODB++ product model name. Default = odbjob. This parameter is required if you want to run the translator without displaying the user interface. See "ODB++Design Entity Naming Rules" on page 46.
-jp <*product_model_path*>	Output Path	Output path for the ODB++ product model. Default = the current working directory. This parameter is required if you want to run the translator without displaying the user interface.
-lp <*log_path*>		Log file path. Default is output product model path.
-m <*tolerance*> -match <*tolerance*>	Symbol tolerance	Where <tolerance> is the number of mils for symbol tolerance. Default = 0.2 inches (200 mils).
-matrix_file <*matrix_path*>	Matrix File	The full path to the matrix file. The matrix file can only be edited from the GUI.
-net_none_flag	Read $NONE$ net	Does not assign the $NONE$ net to features with no net.
-nn -neut_nets	Keep Net names	Nets are renamed to generated numeric values. Default = Net names are kept.
-no_view	Open ODB++Design Viewer	Runs the translator without opening the ODB++Design viewer after the translation has completed.
-noDPW	-	Suppresses automatic launching of the wizard.
-o <*dist*> -outline <*dist*>	Outline size	Where <*dist*> is the number of mils to extend the outline on negative planes. This parameter corresponds to the "-o" option of the Cadence Allegro artwork program. The default value is 0.1 inches (100.0 mils)

Parameter	Equivalent GUI Parameter	Description
-odb_version	ODB++Design version to export job	The ODB++Design version in which to export. • **v8** — ODB++Design Version 8 (default). • **v7** — ODB++ Version 7.
-p <*mode*> -padflash <*mode*>	Padflash	Controls whether Allegro padflash codes are used for padstacks. • **s** (substitute) — substitute padflash definitions using the thermal model file • **i** (ignore) — (default) use the pad size
-p_assem	Export Option = ASSY	Only assembly data is to be written to ODB++ output.
-p_fab	Export Option = FAB	Only fabrication data is to be written to ODB++ output.
-pst <*option*> -profile_symbol_type <*option*>	Symbol type for lines and arcs	Defines the symbol type of lines and arcs describing step profile: r(ound)/s(quare).
-r -read_drc	Import Keepin/ out regions	Triggers the generation of multiple DRC layers beginning with the prefix “drc_”. • Allegro layers Route keepout, Route keepin and Via keepout are used to generate an ODB++ layer called drc_route. • Allegro layers Package keepout, Package keepin, Component keepout and Component keepin are used to create drc_comp_top and drc_comp_bottom. • Allegro layers No_Probe_Top and No_Probe_Bottom are used to create drc_tp_top and drc_tp_bottom.
-ral [<*layer name*>] -rout_artwork_layer [<*layer name*>]	Create Rout From Artwork Layer	Controls how the rout is created: • If <*layer name*> contains the name of a valid layer, as specified in the Allegro artwork, the features in that layer are used to create an ODB++ rout layer with the original name. • If <*layer name*> is empty, or the value is not found in the *.out* files, the translation creates a rout layer by merging the features from the following Allegro artwork CLASS/SUBCLASS: BOARD GEOMETRY:OUTLINE“&”BOARD GEOMETRY:DESIGN_OUTLINE“&”BOARD GEOMETRY:CUTOUT

Parameter	Equivalent GUI Parameter	Description
-rc -round_corners	Round Corners	(Corners of polygons (contours) will be rounded.
-re -remove_eda	Remove EDA Data	Removes EDA component and package data.
-read_sqa <*option*>	Read SQA Data	Controls creation of the signal quality layer. • **yes** — Read SQA data and create an SQA layer. • **no** — (default) Do not read SQA data and create an SQA layer.
-rr <*option*> -read_region <*option*>	Import Areas-Constraint region	**yes** — Generates an ODB++ layer named fab_drc from the Allegro layer group “Constraint region”.
-rrd -remove_dielectric	Remove redundant dielectric	Combines successive dielectric layers.
-sf	Turn eda_cadence_silk_fill on	Set configuration parameter eda_cadence_silk_fill.
-skip_refdes <*option*>	Skip RefDes with Asterisk	Skip components with a RefDes containing an asterisk (*). • **no** — All components are translated. (default) • **yes** — Components with names containing an asterisk are not translated. • **part** — The translation excludes components whose RefDes contains an asterisk but includes their pad and drill features.
-sp	Suppress Unconnected Pads	Sets configuration parameter eda_cadence_suppress.
-te	Turn eda_cadence_therm_err on	Sets configuration parameter eda_cadence_therm_err.
-tf <*thermal_file*>	Use thermal model file	Where <*thermal_file*> is the full path name for the thermal model file. If the thermal_file is specified, the thermal_model must be specified in -tm. If no thermal file is specified, a default model is used, which uses direct connect and no thermals.

Parameter	Equivalent GUI Parameter	Description
-tm <*thermal_model*>	Select Model button	Where <*thermal_model*> is the name of the model to be used. The available model names are defined in the thermal model file. If no thermal_file is specified, the thermal_model is ignored.
-tr_sym		Controls the translation of symbols. • **yes** — Translate symbols as components. If there are multiple shapes with the same name, each will be translated as a separate component. • **no** (default) — Do not translate symbols.
-up -use_panel	Use Panel Outline as profile	Creates the step profile from data with SUBCLASS = DESIGN_OUTLINE/OUTLINE in the *geoms_<pm>.out* file.
-v -ver		Displays version information about the translator. When this option is used, all other parameters are ignored.
-verify		Requests verification from the user before performing various actions such as Save and Translate.

Information Acquired from Cadence Allegro Data

Several types of Cadence Allegro design information stored in the *.out* files are read into the ODB++Design product model. In addition, you can configure the translation to extract specific data that was not imported automatically from a file stored in the base installation location or at an arbitrary path.

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Cadence Allegro DFA Table **83**

Importing Allegro Geometry Properties

You can import geometry properties from the Cadence Allegro design, and store their values in ODB++ user-defined attributes. To do so, you need to create a file that lists the subclasses to extract, and then create a user attribute for each of those subclasses.

Prerequisites

The subclasses associated with the geometry properties that you want to import are stored in the *geoms_<pm>.out* file. See "Generated Extract Files" on page 60.

Procedure

1. Create a file from which to extract the names of the geometry property subclasses:
   a. In a text editor, create a list of the desired subclasses, specifying each subclass on a separate line.

      For example, to import the "Alert" subclass, include this line:

      ```
      Alert
      ```

   b. Do one of the following:
      - Save the list to this file:

        $ALLEGRO_BRD2ODB/added_comp_properties.txt

        Where *$ALLEGRO_BRD2ODB* is the directory where the Siemens product integrated with Cadence Allegro is installed, typically:

        - Valor NPI:

          C:\MentorGraphics\Valor\vNPI_<ver>\edir\get

- ODB++ Inside:

  C:\MentorGraphics\ODB++_INSIDE_CADENCE_ALLEGRO/brd2odb_<ver>

- Save the list as a text file under the name and in the location of your choice.

c. If you saved the geometry properties file to an arbitrary path, set the system environment variable ALLEGRO_GEOM_PROP_BRD2ODB with the full path to this file, including the file name: the subclasses listed here will be extracted during translation.

Note

When the environment variable ALLEGRO_GEOM_PROP_BRD2ODB is set with an explicit path to the component properties file, the *$ALLEGRO_BRD2ODB/added_comp_properties.txt* file is ignored, if it exists.

2. Map the specified geometry property subclasses to ODB++ user attributes:

   a. In a text editor, open the user attributes file as appropriate for your product:

   - Valor NPI:

     $VALOR_DIR/fw/lib/misc/userattr

   - ODB++ Inside:

     $ALLEGRO_BRD2ODB/fw/lib/misc/userattr

   b. For each subclass listed in the geometry properties file, create a user attribute with the appropriate definitions:

   - The Data Type must make logical sense:
     - Text — TEXT
     - True/False — BOOLEAN
     - Integer — INTEGER
     - Float — FLOAT
   - The NAME must be identical to the subclass name, only in lowercase and with an underscore character (_) as a prefix.

     For example, if the subclass name in the geometry file is “Alert,” the NAME definition should be “_alert.”
   - The ENTITY must be “feature.”

The attribute definitions in the following example capture the “Alert” subclass:

```
TEXT {
  NAME=_alert
  PROMPT=Alert
  MIN_LEN=0
  MAX_LEN=100
  ENTITY=feature
  DEF=
  GROUP=Allegro
  OPTIONS=
  DEF_OPT=
}
```

If the attribute definitions are correct for the subclasses specified, a connection is established during translation and the appropriate ODB++ user attributes are assigned to features with the values as defined in Allegro.

Importing Allegro Component Properties

You can import component properties from the Cadence Allegro design as ODB++Design component properties or as user-defined attributes. In each case, you need to create a file that lists the subclasses to be extracted during translation.

Prerequisites

The subclasses associated with the component properties that you want to import are stored in the *geoms_<pm>.out* file. See “Generated Extract Files” on page 60.

Procedure

1. Create a file from which to extract the names of the component property subclasses:
   a. In a text editor, create a list of the desired subclasses, specifying each subclass on a separate line.

      For example, to import the “Description” subclass, include this line:

      ```
      Description
      ```

   b. Do one of the following:
      - Save the list to this file:

        $ALLEGRO_BRD2ODB/added_comp_properties.txt

        Where *$ALLEGRO_BRD2ODB* is the directory where the Siemens product integrated with Cadence Allegro is installed, typically:

        - Valor NPI:

          C:\MentorGraphics\Valor\vNPI_<ver>\edir\get

- ODB++ Inside:

  C:\MentorGraphics\ODB++_INSIDE_CADENCE_ALLEGRO/brd2odb_<ver>

- Save the list as a text file under the name and in the location of your choice.

c. If you saved the component properties file to an arbitrary path, set the system environment variable ALLEGRO_COMP_PROP_BRD2ODB with the full path to this file, including the file name: the subclasses listed here will be extracted during translation.

Note

When the environment variable ALLEGRO_COMP_PROP_BRD2ODB is set with an explicit path to the component properties file, the *$ALLEGRO_BRD2ODB/added_comp_properties.txt* file is ignored, if it exists.

Tip

If you want the data in the specified subclasses to be imported to ODB++Design as component properties rather than component attributes, you are done and do not need to continue with the rest of this procedure.

2. (Optional) Map the specified component property subclasses to ODB++ user attributes:

   a. In a text editor, open the user attributes file as appropriate for your product:

   - Valor NPI:

     $VALOR_DIR/fw/lib/misc/userattr

   - ODB++ Inside:

     $ALLEGRO_BRD2ODB/fw/lib/misc/userattr

   b. For each subclass listed in the component properties file, create a user attribute with the appropriate definitions:

   - The Data Type must make logical sense:
     - Text — TEXT
     - True/False — BOOLEAN
     - Integer — INTEGER
     - Float — FLOAT
   - The NAME must be identical to the subclass name, only in lowercase and with an underscore character (_) as a prefix.

     For example, if the subclass name in the geometry file is “Description,” the NAME definition should be “_description.”

- The ENTITY must be “component.”

The attribute definitions in the following example capture the “Description” subclass:

```
TEXT {
  NAME=_description
  PROMPT=Description
  MIN_LEN=0
  MAX_LEN=100
  ENTITY=component
  DEF=
  GROUP=Allegro
  OPTIONS=
  DEF_OPT=
}
```

If the attribute definitions are correct for the subclasses specified, a connection is established during translation and the appropriate ODB++ user attributes are assigned to components with the values as defined in Allegro.

Deriving Component Outline From Specific Subclasses

You can import data in specific component subclasses as the component outline. To do so, you need to create a file that lists the subclasses to extract, and then specify those subclasses in the Additional Parameters dialog box during translation.

Prerequisites

To be properly associated with the packages on the board, the component subclasses must be part of the Package Geometry class and must be added at the library level.

Procedure

1. Using a text editor, specify the two subclasses in which the top and bottom component outlines are stored, as defined in Allegro. Put each name on a separate line, for example:

   ```
   DISPLAY_TOP
   DISPLAY_BOTTOM
   ```

2. Do one of the following:

   - Save the list to this file:

     $ALLEGRO_ BRD2ODB/added_comp_subclasses.txt

Where *$ALLEGRO_ BRD2ODB* is the directory where the Siemens product integrated with Cadence Allegro is installed, typically:

- Valor NPI:

  C:\MentorGraphics\Valor\vNPI_<ver>\edir\get

- ODB++ Inside:

  C:\MentorGraphics\ODB++_INSIDE_CADENCE_ALLEGRO/brd2odb_<ver>

- Save the list as a text file under the name and in the location of your choice.

3. If in the previous step you saved the component subclasses file to an arbitrary path, set the system environment variable ALLEGRO_COMP_SUBCLASSES_BRD2ODB with the full path to this file, including the file name: the subclasses listed here will be used during translation.

Note

When the environment variable ALLEGRO_COMP_SUBCLASSES_BRD2ODB is set with an explicit path to the component subclasses file, the *$ALLEGRO_ BRD2ODB/added_comp_subclasses.txt* file is ignored, if it exists.

Results

Running the translation with the additional parameter Component Outline = User Defined and the names of the subclasses in the component subclasses file specified in the User Defined Top and User Defined Bottom fields sets the component outline with the data in those subclasses.

Examples

Figure 2-1. Setting Component Outline to DISPLAY_TOP and DISPLAY_BOTTOM (Subclasses) in Valor NPI

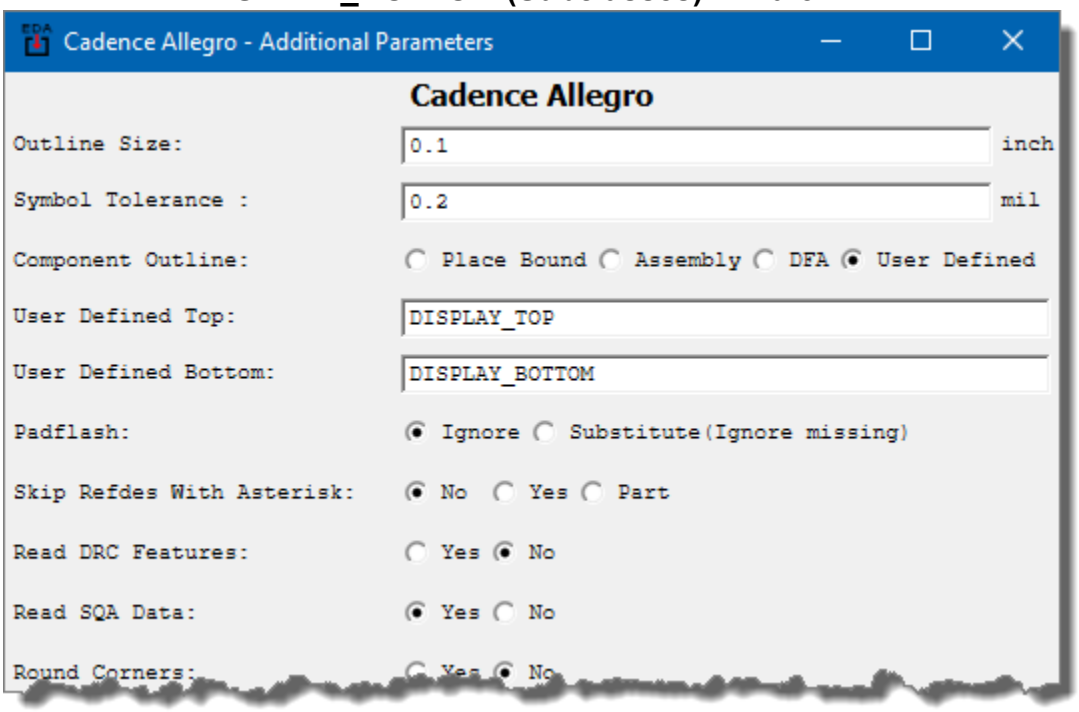
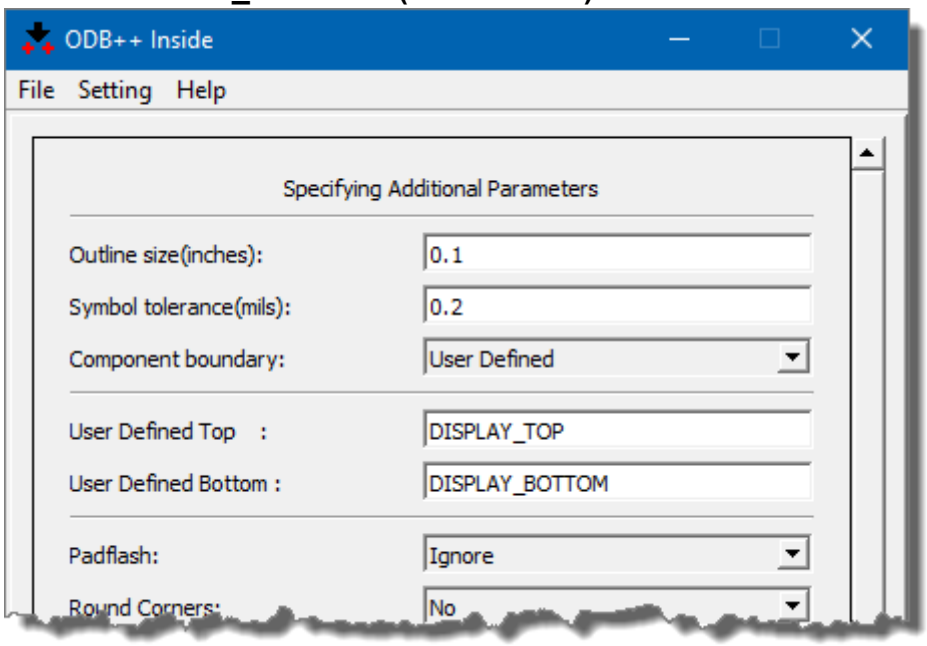


Figure 2-2. Setting Component Outline to DISPLAY_TOP and DISPLAY_BOTTOM (Subclasses) in ODB++ Inside



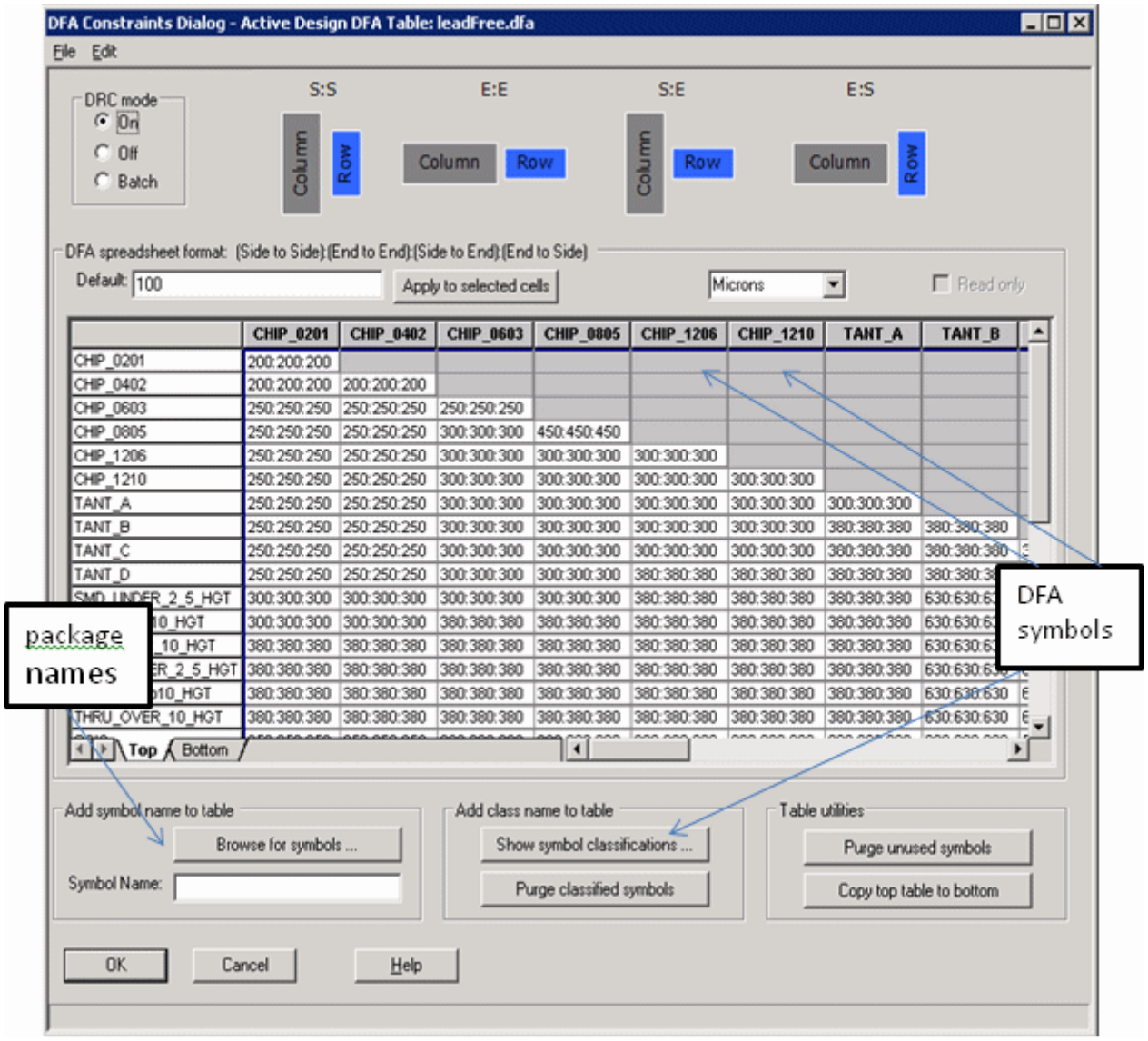
Cadence Allegro DFA Table

The DFA table defines the distance required between different types of components. If the design contains this table, the information is extracted according to the Cadence Allegro version, and then imported into the product model.

DFA Table Versions Prior to 17.4

Access: Click **DFA** () in the toolbar.

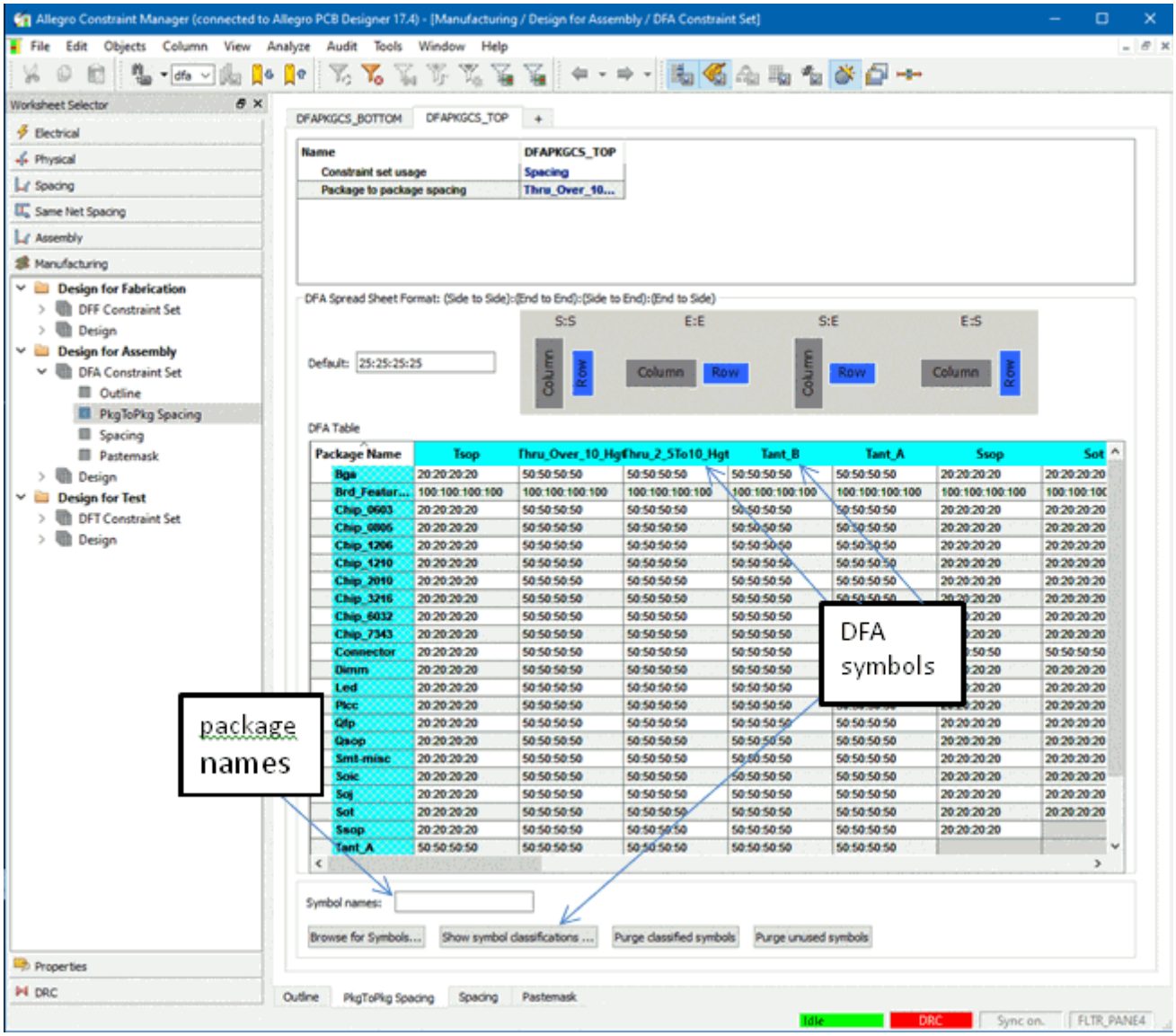
Data extracted to: *dfa_<pm>.out*.



DFA Table Versions 17.4 and Newer

Access: In the Worksheet Selector pane, choose **Manufacturing > Design for Assembly > DFA Constraint Set > PkgToPkg Spacing**.

Data extracted to: *tech_<pm>.out*.



Related Topics

Generated Extract Files

Supported Features

These features are included in the translator.

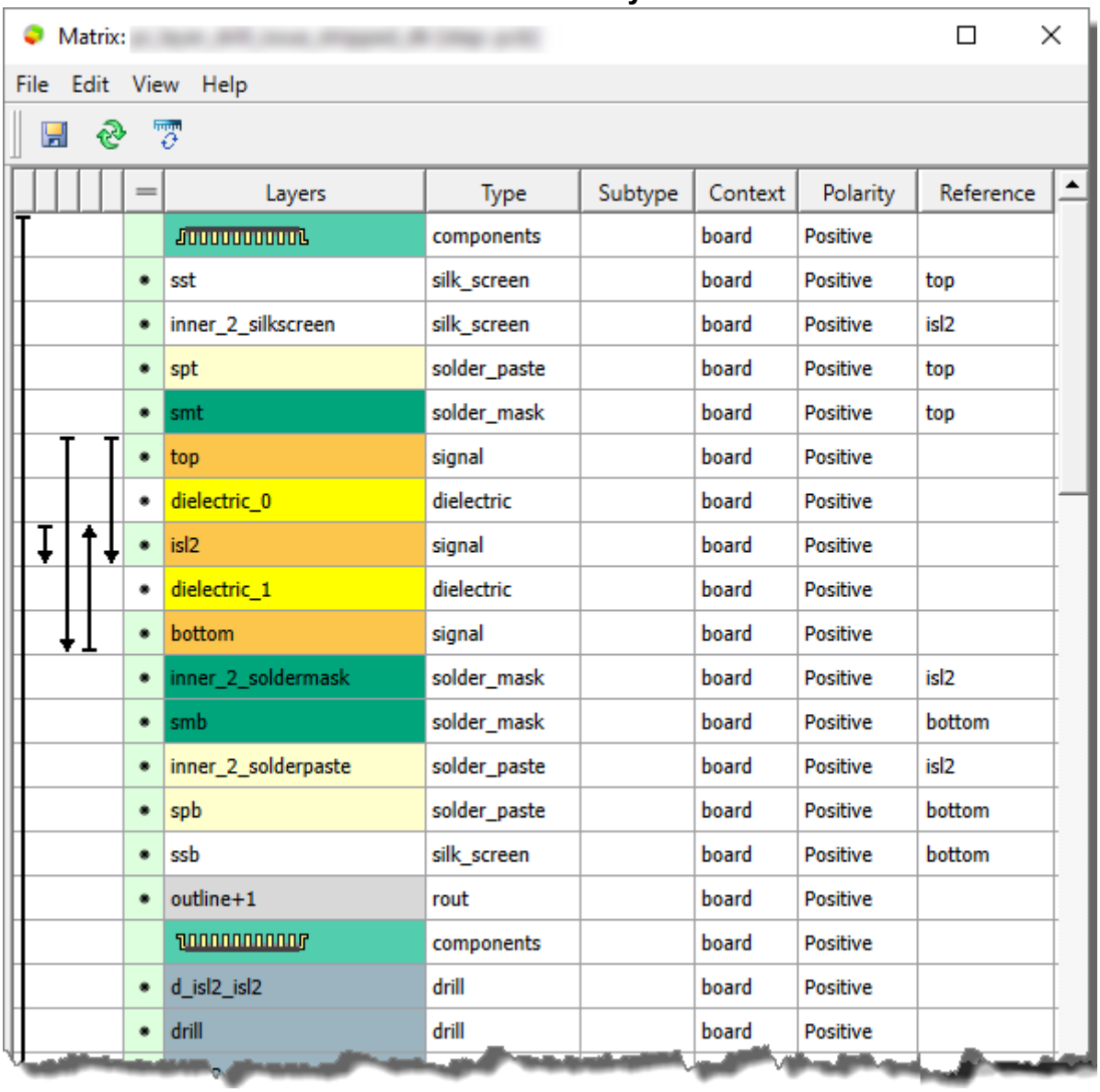
Support for Mask Layers Associated With Inner Copper Layers 85
Support for Padstack Types and Usage 87
Support for Test Point Shapes 87
Support for Intentional Shorts 87
Support for Components Excluded From BOM 87
Support for DFA Boundaries 88
Support for Partial ODB++Design Output 88
Support for Flex Subtypes 88
Support for Boundary Elements 88
Support for Backdrill Size 88
Support for Dielectric Layer Subtypes 89
Support for Bend Areas 89
Support for Skipping Extraction of Net Impedance Average 89
Package Height Properties 89
Support for CLASS_CONSTRAINT_REGION 97
Support for Translating Back-Drill Information 97
Support for Mirrored Padstacks 97
Support for the COMPONENT KEEPOUT Class 97

Support for Mask Layers Associated With Inner Copper Layers

The Type, Context, and Reference parameters of the solder mask, solder paste, and silk screen layers associated with inner copper layers are now set in a post-process function, based on the definitions in the films file.

In the resulting ODB++Design matrix, these layers are grouped by type and positioned above or below the copper layers, according to the side of their associated components. The order of layers in a group reflects the order of their reference copper layers.

Figure 2-3. ODB++Design Matrix With Inner Solder Paste, Silk Screen, and Solder Mask Layers



Layers	Type	Subtype	Context	Polarity	Reference
	components		board	Positive	
sst	silk_screen		board	Positive	top
inner_2_silkscreen	silk_screen		board	Positive	isl2
spt	solder_paste		board	Positive	top
smt	solder_mask		board	Positive	top
top	signal		board	Positive	
dielectric_0	dielectric		board	Positive	
isl2	signal		board	Positive	
dielectric_1	dielectric		board	Positive	
bottom	signal		board	Positive	
inner_2_soldermask	solder_mask		board	Positive	isl2
smb	solder_mask		board	Positive	bottom
inner_2_solderpaste	solder_paste		board	Positive	isl2
spb	solder_paste		board	Positive	bottom
ssb	silk_screen		board	Positive	bottom
outline+1	rout		board	Positive	
	components		board	Positive	
d_isl2_isl2	drill		board	Positive	
drill	drill		board	Positive	

Inner solder mask and solder paste layers connected to components on both sides are placed on the top side of the board.

The side of the inner silk screen layers for which no component reference exists is determined by the Mirrored flag in the EDA data.

See “Generated Extract Files” on page 60.

Support for Padstack Types and Usage

Hole type and padstack usage data is read in from the *padstacks_<pm>.out* file and the associated attributes are added to the design.

See "Generated Extract Files" on page 60.

Support for Test Point Shapes

The translator now places test point shapes on dedicated top and bottom documentation layers that have the same name as in Cadence Allegro.

The location and graphical representation of a test point shape are read into the TEST_POINT and PROBE_FIGURE fields of the *pins_<pm>.out* file.

See "Generated Extract Files" on page 60.

Support for Intentional Shorts

The translator now reads in intentional shorts data from Cadence. Known shorts are not reported as violations in Valor NPI Netlist Analyzer.

Shorted nets information is extracted to the NET_SHORT field of the *pins_<pm>.out* and *geoms_<pm>.out* files, where the former provides the values for pins and vias, and the latter for SMD pads. During translation, these values are used to define the intentional short instances in the *<step_name>/eda/shortf* file.

See "Generated Extract Files" on page 60.

Support for Components Excluded From BOM

The translator supports components marked as "BOM ignored" in Cadence Allegro.

Components with BOM_IGNORE data are assigned the following attributes during translation:

- **Not Populated per BOM** (.no_pop) — Designates the component as being not populated for the current version of the BOM.
- **Ignore Graphically/Output** (.comp_ignore) — Designates the component as to be ignored when calculating statistics, or during certain operations, such as analysis.

See "*comps_<pm>.out*" file "Generated Extract Files" on page 60.

Support for DFA Boundaries

The translator supports the DFA_BOUND_TOP and DFA_BOUND_BOTTOM sub-classes for the PART GEOMETRY class.

You can configure the translation to derive the component outline from the respective fields of the components file by setting the "Component Outline" parameter as described in "Specifying Additional Parameters Pages" on page 21.

Support for Partial ODB++Design Output

The translator supports partial ODB++ output.

ODB++Design Inside for Cadence Allegro now supports partial output based on a layer groups list. See "Specifying Partial Export Parameters Page" on page 19.

Support for Flex Subtypes

The translator supports flex subtypes.

The copper layers below and above the dielectric layer whose LAYER_MATERIAL definition in the *layers_<pm>.out* file matches one of the flexible dielectric material names listed for the configuration parameter eda_flex_material, are assigned the appropriate flex subtypes. See "Subtypes to Support Flex/Rigid Flex Manufacturing" in *Getting Started With ODB++Design*.

See "Generated Extract Files" on page 60.

Support for Boundary Elements

The translator reads in boundary elements to a documentation layer.

Boundary elements are surface areas used to create copper etch automatically within Allegro. If configuration parameter eda_cadence_add_boundary_layer = yes, a documentation layer is created for each record with in the *geoms_<pm>.out* file with CLASS = BOUNDARY, using this naming convention: *boundary_<layer_name>*.

Support for Backdrill Size

The translator supports backdrill size.

Backdrill size is read from the corresponding field in the *pins_<pm>.out* file. If this field does not exist, the drill padstack definition is the backdrill size. See "Generated Extract Files" on page 60.

Support for Dielectric Layer Subtypes

The translator supports Layer Subtypes for prepreg and core dielectric layers.

Layer Subtype for dielectric layers is read from the LAYER_FUNCTION field of the *layers_<pm>out* file:

- **LAYER_FUNCTION = DIELECTRIC_CORE** — Layer Subtype = core
- **LAYER_FUNCTION = DIELECTRIC_PREPEG** — Layer Subtype = prepreg
- **LAYER_FUNCTION ≠ DIELECTRIC_CORE, DIELECTRIC_PREPEG** — No Layer Subtype is provided

Support for Bend Areas

The translator supports bend areas.

If the Cadence Allegro design contains bend areas, this information is stored in the ODB++ product model in a layer named bend_area. This is a positive board layer of type mask and subtype bend_area. Bend area information is used in rigid flex analysis.

Support for Skipping Extraction of Net Impedance Average

During export from Allegro, the attribute NET_IMPEDANCE_AVERAGE is calculated for each net.

The *valor_ext.il* import script prompts for permission to skip this time consuming calculation, if the information is not required. As a result, extraction time is reduced.

Package Height Properties

Cadence Allegro properties package_height_min and package_height_max are interpreted to match their meaning in Cadence Allegro.

The usage of each of the properties depends on whether the other property is defined.

- **package_height_max** — The height of the component.

  This is stored in the ODB++ component attribute .comp_height (Height).

  The property package_height_max is not considered when package_height_min is specified.

If package_height_min is not specified, package_height_max is used to indicate whether all components or no components can be placed in the area, regardless of their height:

- **package_height_max = 0** — Any components can be placed in this area.
- **package_height_max0** — No components can be placed in this area.

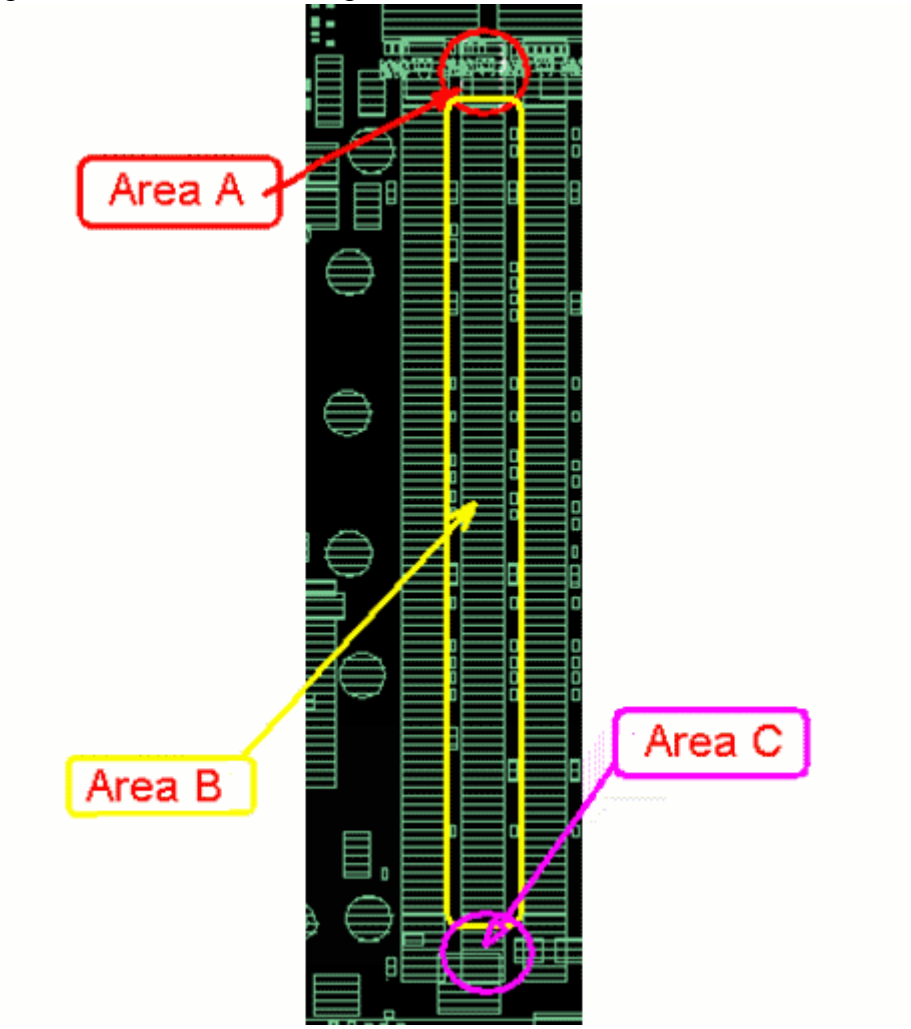
- **package_height_min** — The amount of space under the component. This is the lower limit of the height of the keepout area. If this value is specified for a keepout area, only components with height less than this value can be placed in this area.

  If a component is defined in Allegro as having a value for property package_height_min or if there are areas of the component with values for package_height_min, this information is stored with the product model, and can be used during component analysis.

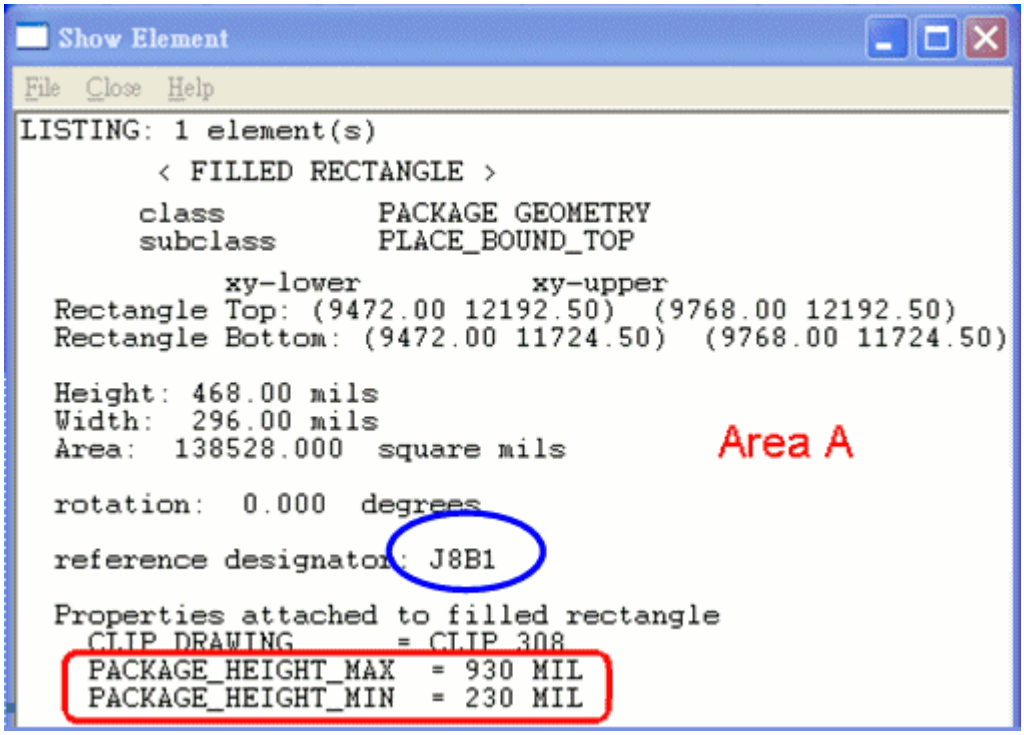
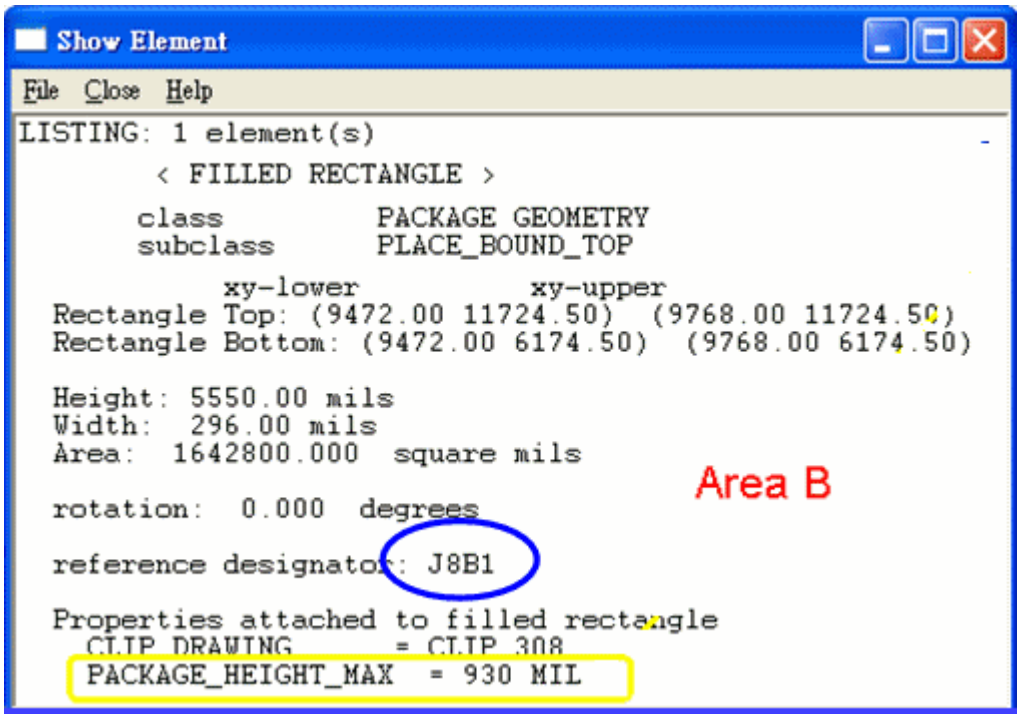
  A layer (height_top) is created in ODB++ to store height information for areas where there is space underneath components. In this layer, the maximum height of components that can be placed in a particular area is defined in the ODB++ feature attribute .drc_max_height (Maximum Height for Component). This attribute is set to the value of package_height_min for components, or for areas of components, where package_height_min is specified.

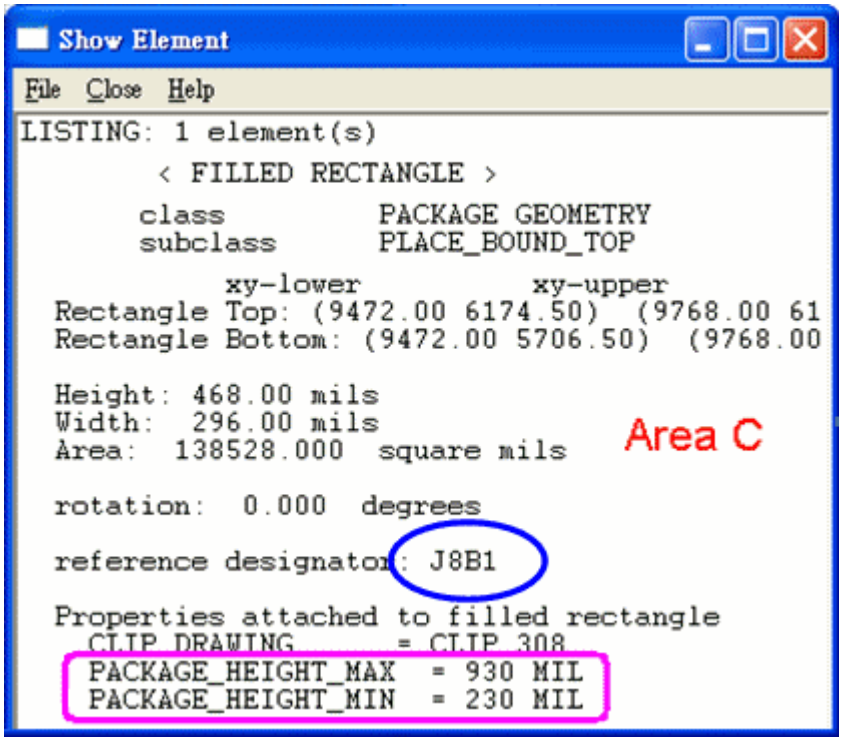
Example of a Component With Multiple Areas

In the example, RefDes J8B1 is a component with three areas defined.



These are the areas as defined in Cadence Allegro:

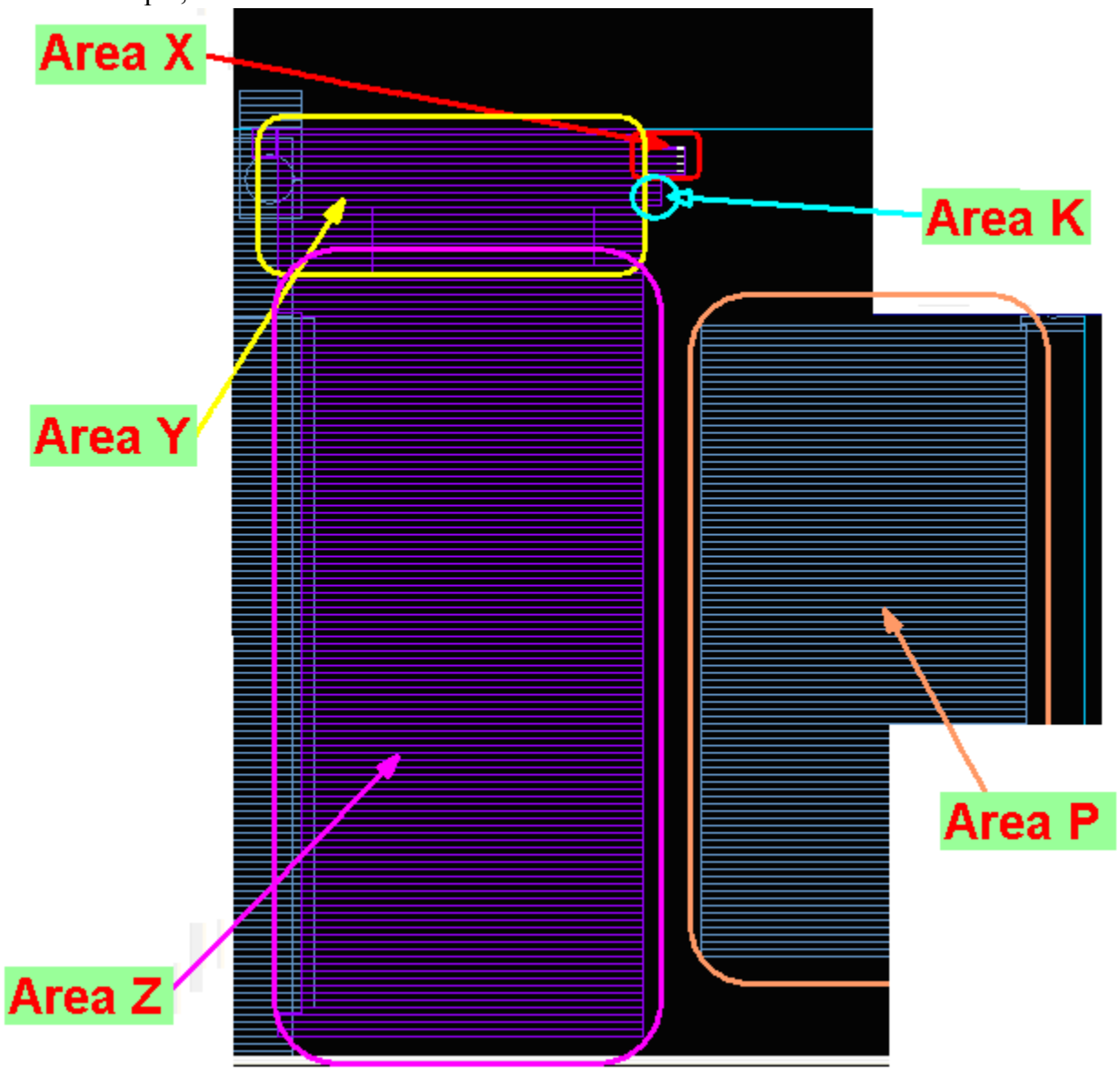
Area	Definition
Area A	
Area B	

Area	Definition
Area C	

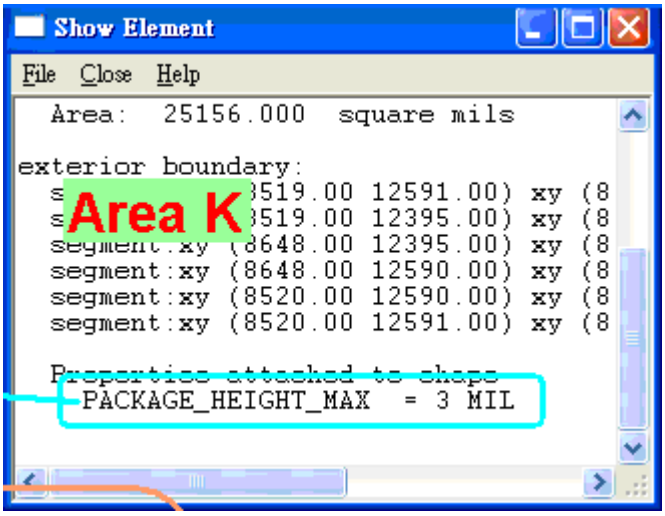
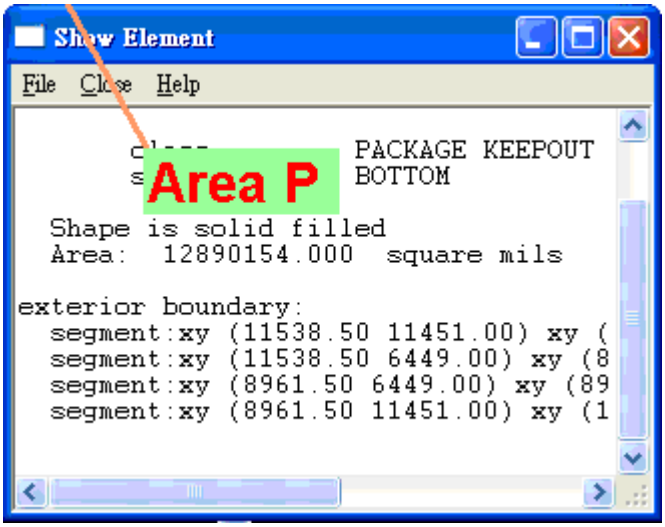
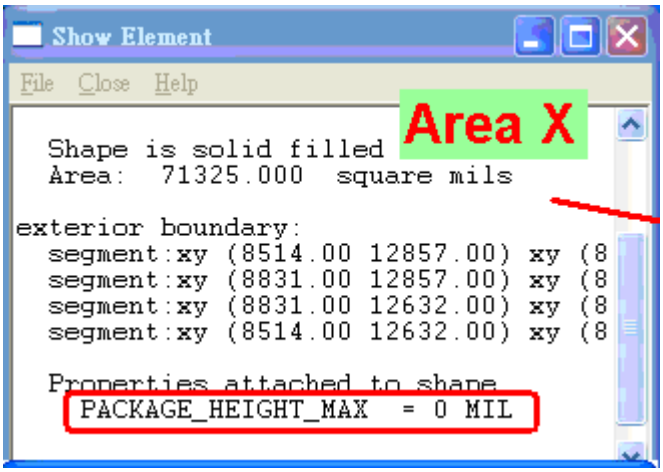
- The main part of the component (Area B in the example) is resting on the board, so it has no value for package_height_min.
- At the two ends of the component (Area A and Area C in the example), there is a space of height 230 mil underneath. A component that is placed under an end area of this component is not reported as an error if its height is less than 230 mil.

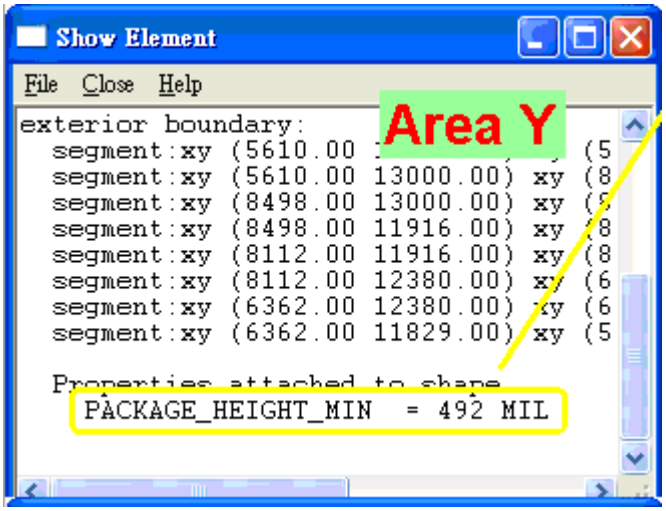
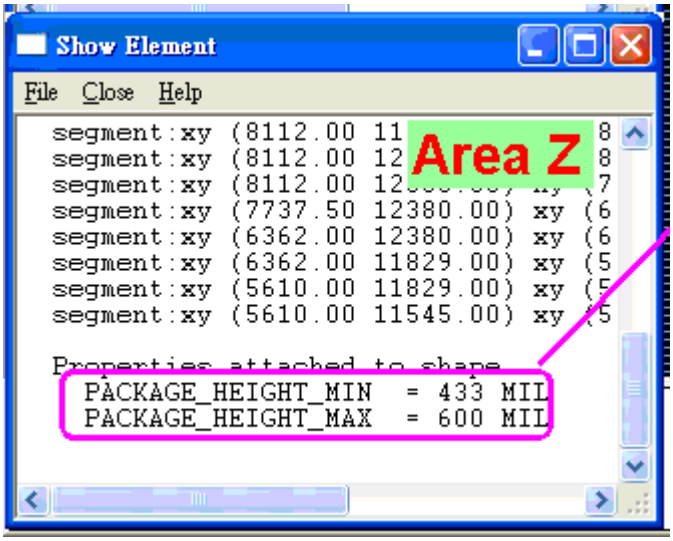
Example of Keepout Areas Based on Package Height Properties

In the example, several areas are defined.



These are the areas as defined in Cadence Allegro:

Area	Definition
Area K	
Area P	
Area X	

Area	Definition
Area Y	
Area Z	

The example shows these areas:

Area	package_height_min	package_height_max	Components Allowed	Description
X	not specified	0	all	package_height_max = 0
Y	492 mil	not specified	height < 492 mil	
Z	433 mil	600 mil	height < 433 mil	package_height_max is not considered when package_height_min is specified.
K	not specified	3 mil	none	package_height_max > 0
P	not specified	not specified	none	Neither property is specified.

Support for CLASS_CONSTRAINT_REGION

ODB++Design Inside for Cadence Allegro supports class type CLASS_CONSTRAINT_REGION that was added to Cadence Allegro version 16.

Support for Translating Back-Drill Information

If the Cadence Allegro design contains back-drill information, new drill layers are created, for each drill span, to include this information.

Recent versions of Cadence Allegro implement back-drilling via the net property BACKDRILL_MAX_PTH_STUB, with the value denoting the maximum depth of the back-drill.

During translation, backdrills are added for pins/via holes and to existing drills. The span cannot be from top to bottom but must start or end with the top/bottom. A new layer is added for each backdrill span.

Support for Mirrored Padstacks

If a via is mirrored, or if a pin is used for a component on the bottom of the board, padstack information is taken from the mirrored layer.

Support for the COMPONENT KEEPOUT Class

The COMPONENT KEEPOUT class works like the PACKAGE KEEPOUT class.